

Compal Confidential

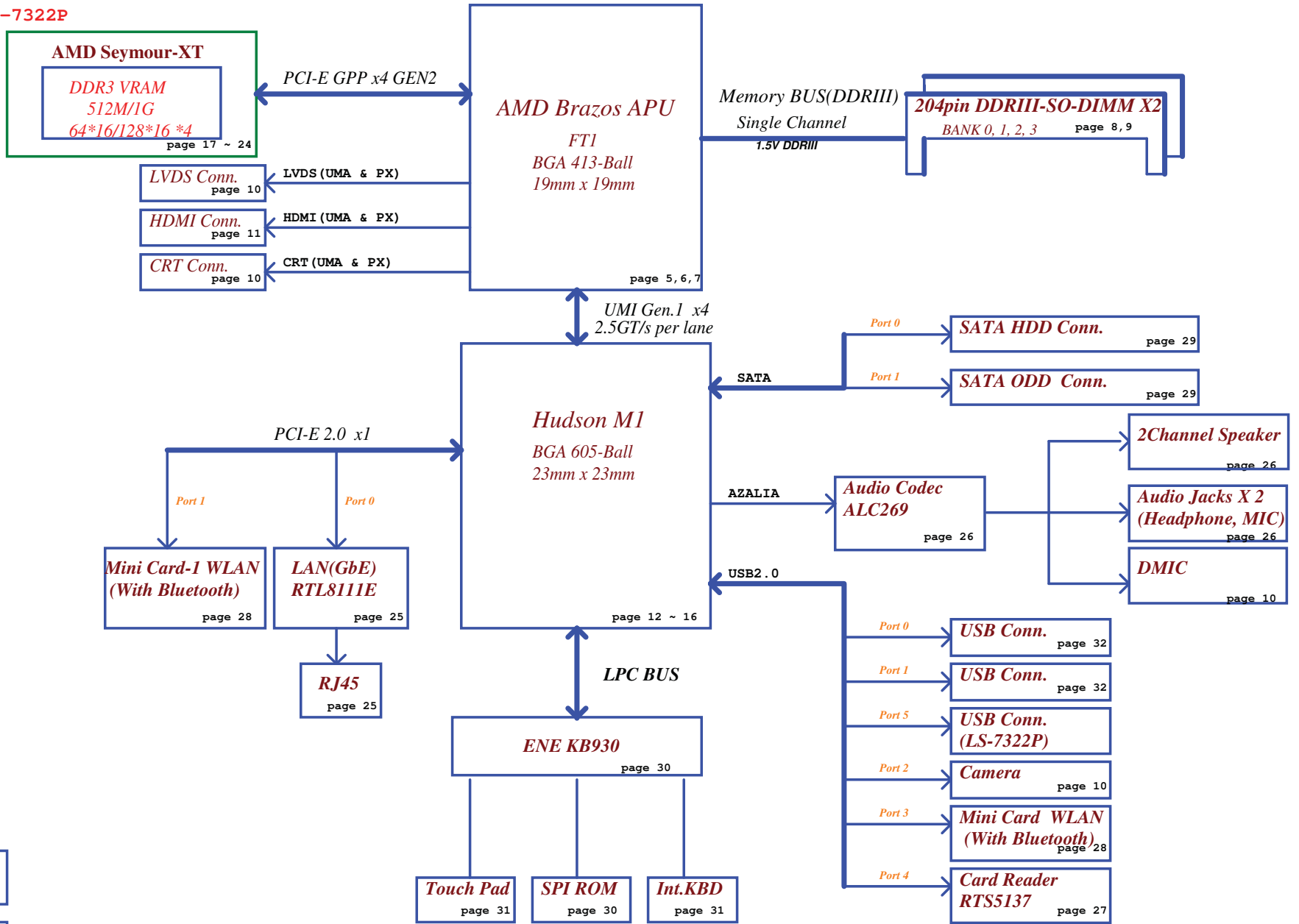
PBL60 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

2010-02-15

REV: 1.0

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LS-7326P
Power BD

LS-7322P
Audio BD

Thermal Sensor
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH (+3VS)	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	FCH (+3VALW)	X	X	V	X	X	X

FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

SCL0, SDA0 (Primary SMBUS in the S0 domain)
 SCL1, SDA1 (Secondary SMBUS supporting ASF)
 SCL2, SDA2 (Primary SMBUS in the S5 domain)
 SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
 SCL4, SDA4 (Primary SMBUS in the S5 domain)

L01 : 16G@/VGA@/LS@/X76@L03

L02 : 16G@/UMA@/LS@

L03 : 15G@/VGA@/LS@/X76@L03

L04 : 15G@/UMA@/LS@

L05 : 16G@/VGA@/LS@/X76@L01



L06 : 15G@/VGA@/LS@/X76@L01

L07 : 1G@/VGA@/LS@/X76@L03

L08 : 1G@/UMA@/LS@

L09 : 1G@/VGA@/LS@/X76@L01

Symbol Note :

 : means Digital Ground
 : means Analog Ground

BOM Structure

15G@ : 1.5G CPU (E240)
 16G@ : 1.6G CPU (E350)
 1G@ : 1G CPU (C50)
 UMA@ : APU output.
 VGA@ : GPU used.
 LS@ : Level shift used.
 X76@L01 : VRAM 1G.
 X76@L03 : VRAM 512M.

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Power-Up/Down Sequence

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDR3 should ramp-up before or simultaneously with VDDC.
- For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
- The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VSG)

PCIE_VDDC(1.0V)

VDDR1(1.5VSG)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

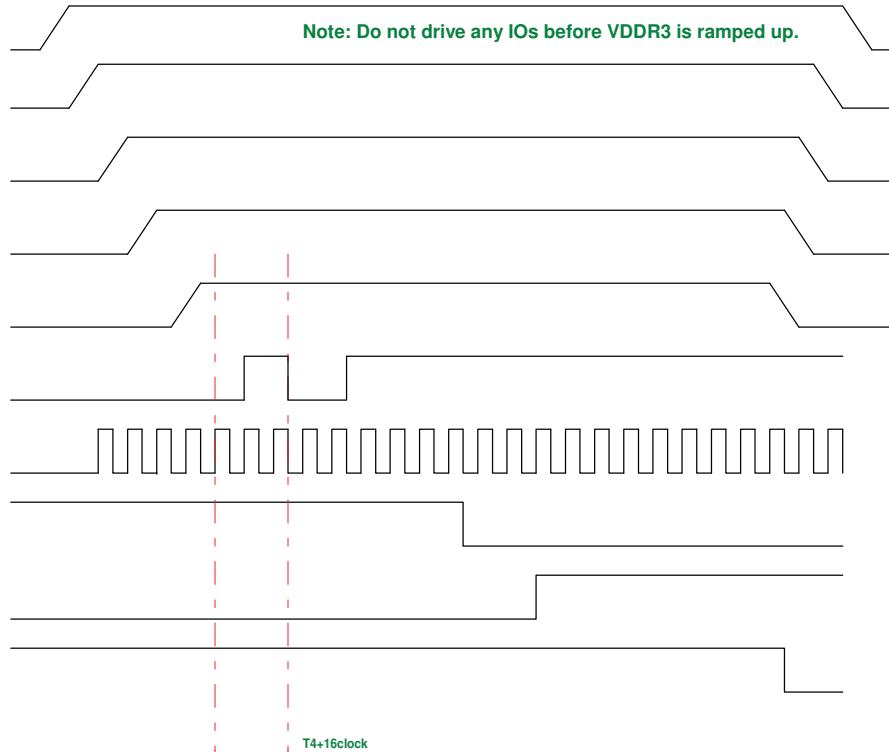
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset



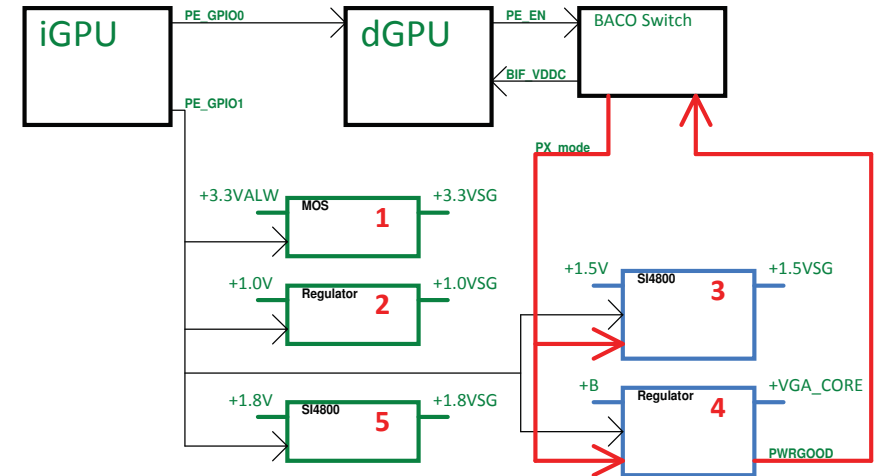
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

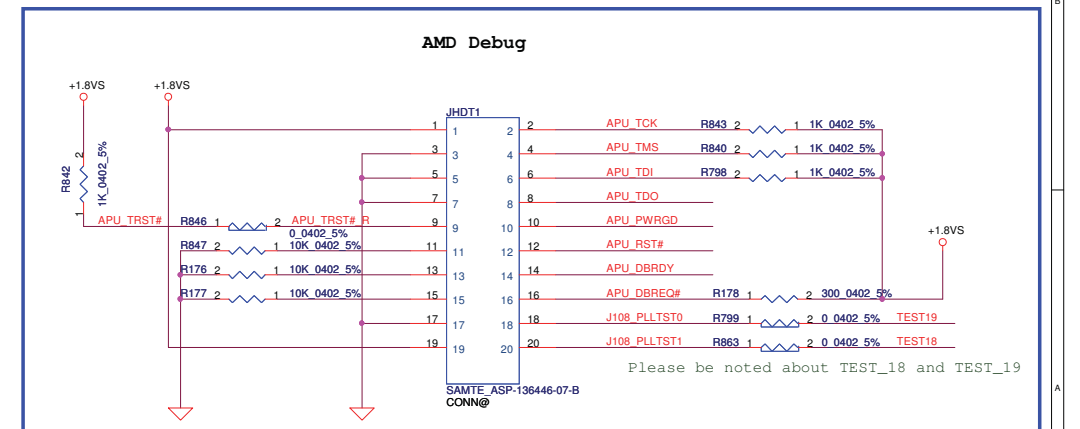
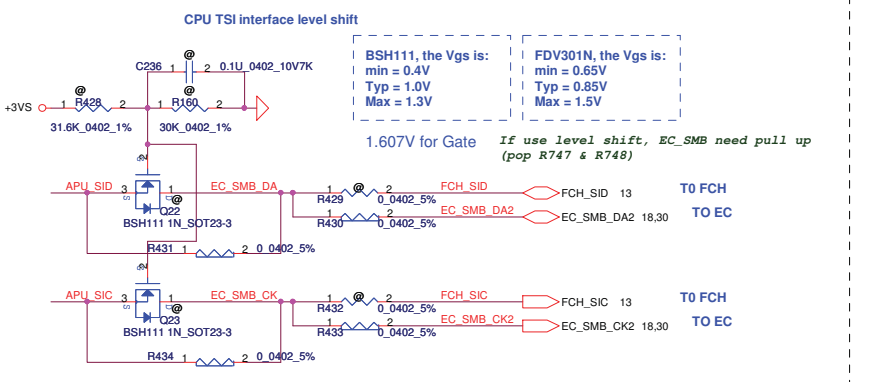
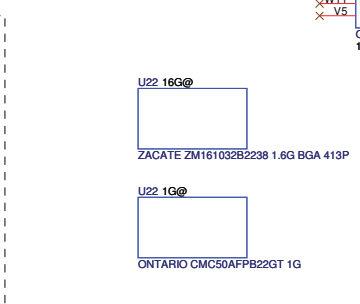
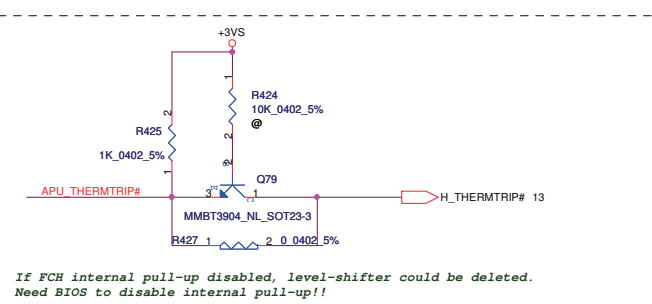
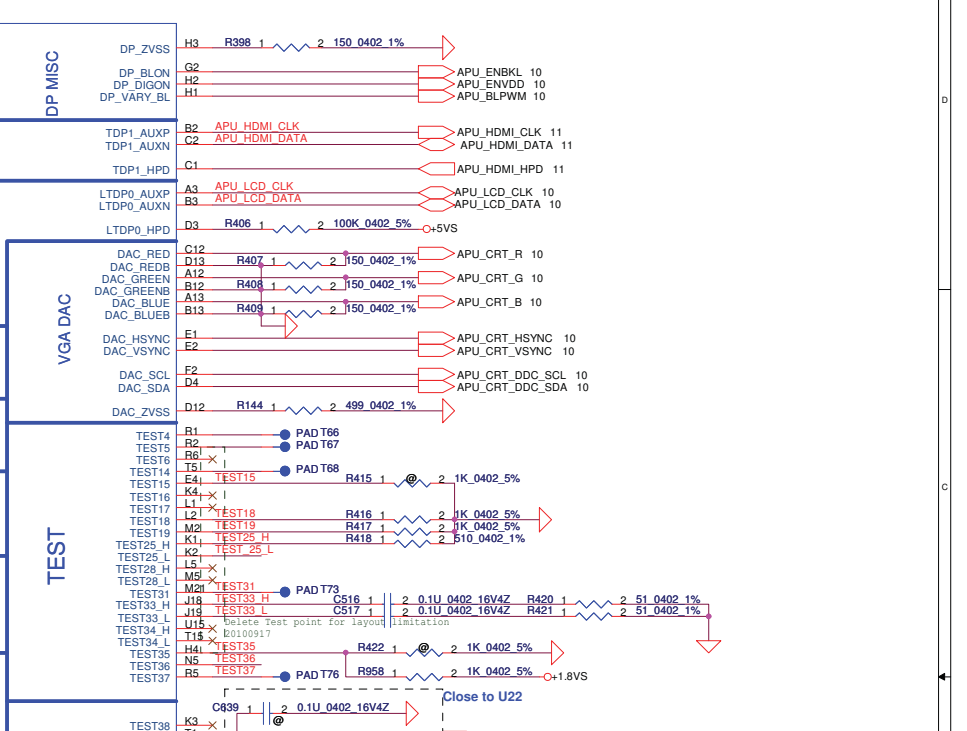
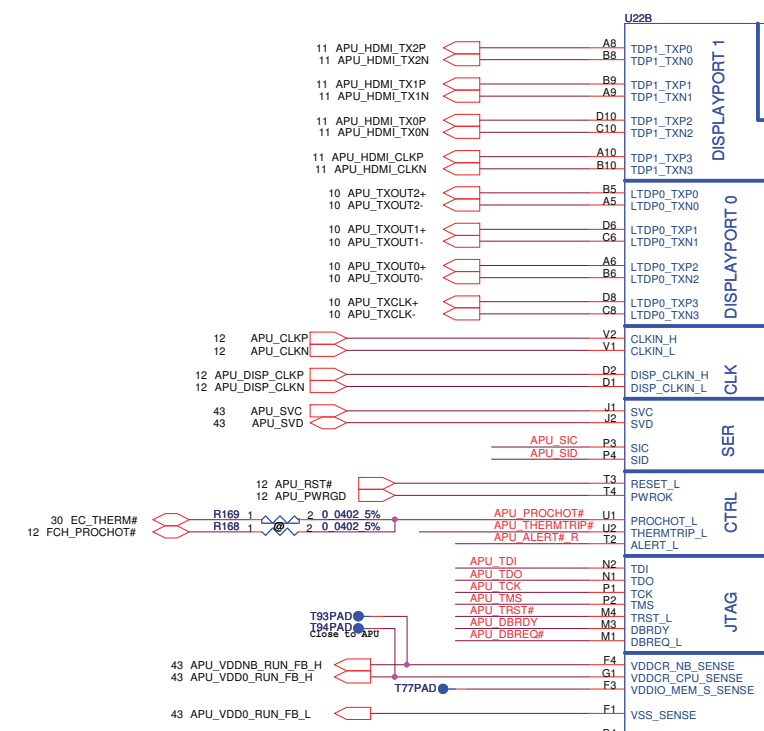
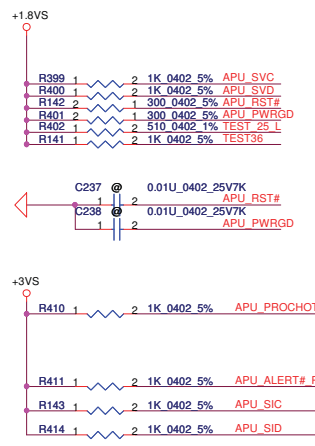
BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



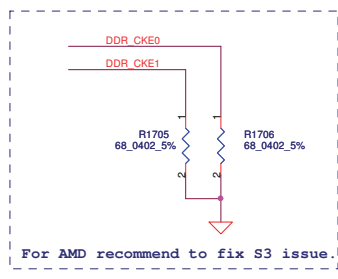
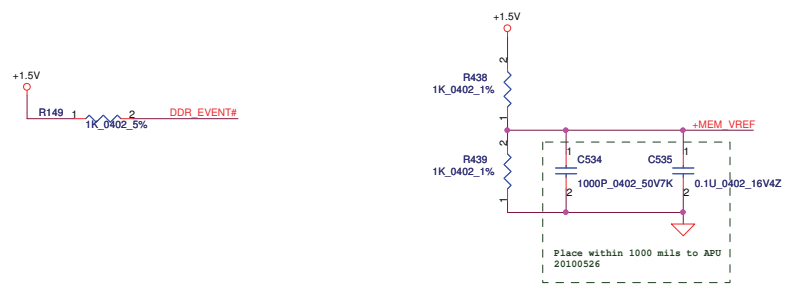
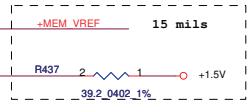
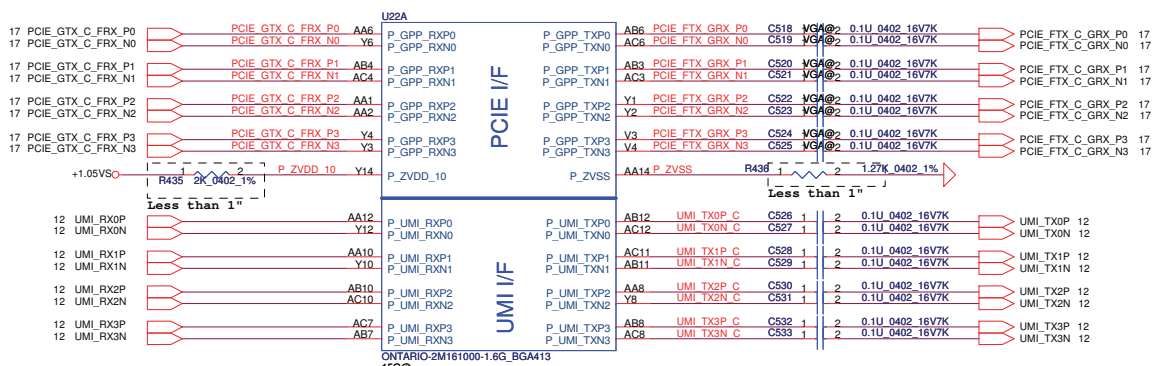
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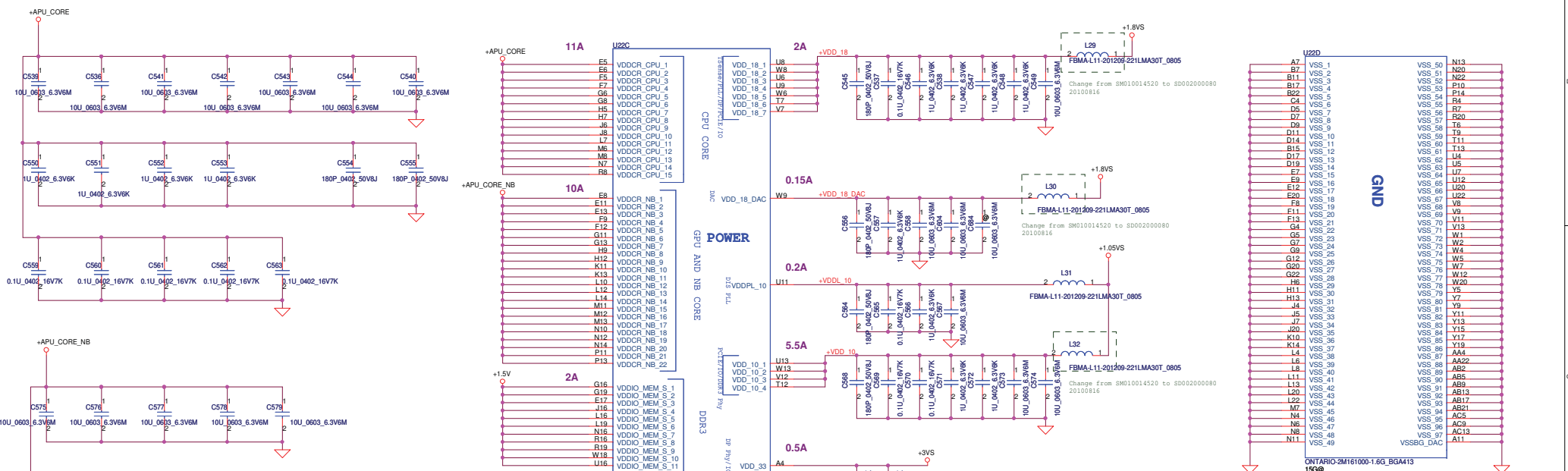
U22E			
DDR_A_MA0	R17	M_ADD0	B14
DDR_A_MA1	H19	M_ADD1	A15
DDR_A_MA2	J17	M_ADD2	A17
DDR_A_MA3	H18	M_ADD3	D18
DDR_A_MA4	G17	M_ADD4	A14
DDR_A_MA5	H17	M_ADD5	C14
DDR_A_MA6	H15	M_ADD6	C16
DDR_A_MA7	G18	M_ADD7	D16
DDR_A_MA8	E19	M_ADD8	C18
DDR_A_MA9	E19	M_ADD9	A19
DDR_A_MA10	T19	M_ADD10	B21
DDR_A_MA11	F17	M_ADD11	D20
DDR_A_MA12	E18	M_ADD12	A18
DDR_A_MA13	W17	M_ADD13	B18
DDR_A_MA14	E16	M_ADD14	A21
DDR_A_MA15	G15	M_ADD15	C20
8.9 DDR_A_BS0	B18	M_BANK0	C23
8.9 DDR_A_BS1	T18	M_BANK1	D23
8.9 DDR_A_BS2	F16	M_BANK2	F23
	D15	M_DM0	F22
	B19	M_DM1	C22
	D21	M_DM2	D22
	H22	M_DM3	F21
	P23	M_DM4	H21
	V23	M_DM5	H23
	AB20	M_DM6	K22
	AA16	M_DM7	K21
8.9 DDR_A_DQS0	A16	M_DQS_H0	H20
8.9 DDR_A_DQS#0	B16	M_DQS_L0	H20
8.9 DDR_A_DQS1	B20	M_DQS_H1	H20
8.9 DDR_A_DQS#1	A20	M_DQS_L1	H20
8.9 DDR_A_DQS2	E23	M_DQS_H2	H20
8.9 DDR_A_DQS#2	E22	M_DQS_L2	H20
8.9 DDR_A_DQS3	J22	M_DQS_H3	H20
8.9 DDR_A_DQS#3	J23	M_DQS_L3	H20
8.9 DDR_A_DQS4	R22	M_DQS_H4	H20
8.9 DDR_A_DQS#4	P22	M_DQS_L4	H20
8.9 DDR_A_DQS5	W22	M_DQS_H5	H20
8.9 DDR_A_DQS#5	V22	M_DQS_L5	H20
8.9 DDR_A_DQS6	AC20	M_DQS_H6	H20
8.9 DDR_A_DQS#6	AC21	M_DQS_L6	H20
8.9 DDR_A_DQS7	AB16	M_DQS_H7	H20
8.9 DDR_A_DQS#7	AC16	M_DQS_L7	H20
9 DDR_A_CLK0	M17	M_CLK_H0	Y21
9 DDR_A_CLK#0	M16	M_CLK_L0	Y21
9 DDR_A_CLK1	M19	M_CLK_H1	Y21
9 DDR_A_CLK#1	M18	M_CLK_L1	Y21
8 DDR_B_CLK2	N18	M_CLK_H2	Y21
8 DDR_B_CLK#2	N19	M_CLK_L2	Y21
8 DDR_B_CLK3	L18	M_CLK_H3	Y21
8 DDR_B_CLK#3	L17	M_CLK_L3	Y21
8.9 DDR_RST#	L23	M_RESET_L	Y20
8.9 DDR_EVENT#	N17	M_RESET_L	Y20
8.9 DDR_CKE0	F15	M_CKE0	Y18
8.9 DDR_CKE1	E15	M_CKE1	Y18
9 DDR_A_ODT0	W19	M0_ODT0	Y16
9 DDR_A_ODT1	V15	M0_ODT1	Y16
8 DDR_B_ODT0	U19	M1_ODT0	Y16
8 DDR_B_ODT1	W15	M1_ODT1	Y16
9 DDR_CS0_DIMMA#	T17	M0_CS_L0	Y16
9 DDR_CS1_DIMMA#	W16	M0_CS_L1	Y16
8 DDR_CS0_DIMMB#	U17	M1_CS_L0	Y16
8 DDR_CS1_DIMMB#	V16	M1_CS_L1	Y16
8.9 DDR_A_RAS#	U18	M_RAS_L	Y16
8.9 DDR_A_CAS#	V19	M_CAS_L	Y16
8.9 DDR_A_WE#	V17	M_WE_L	Y16

DDR SYSTEM MEMORY



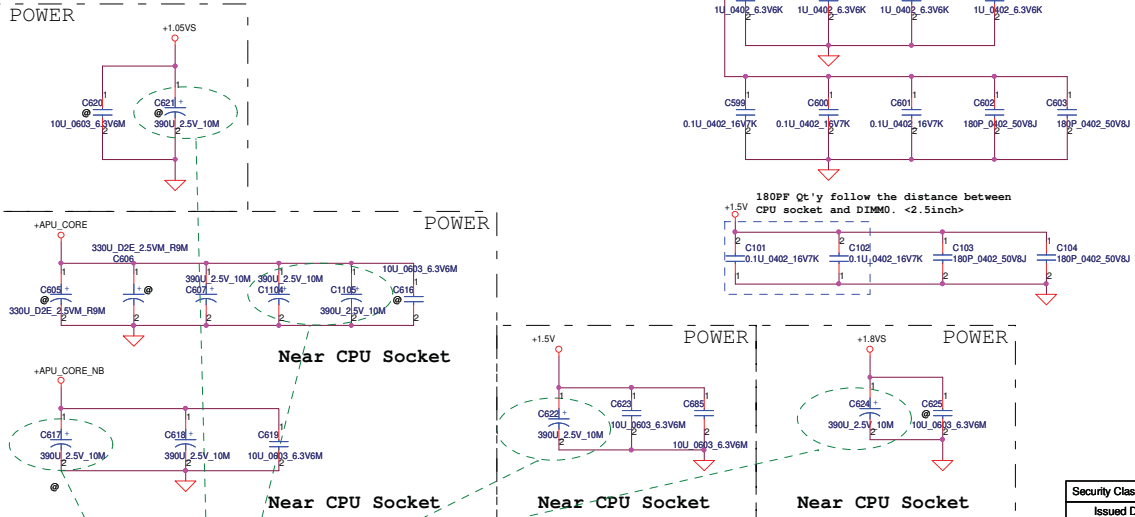
For AMD recommend to fix S3 issue.

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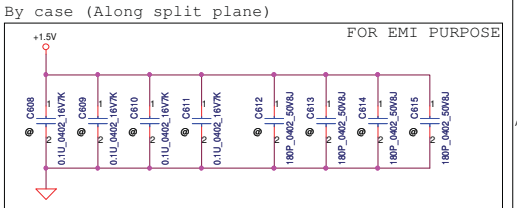


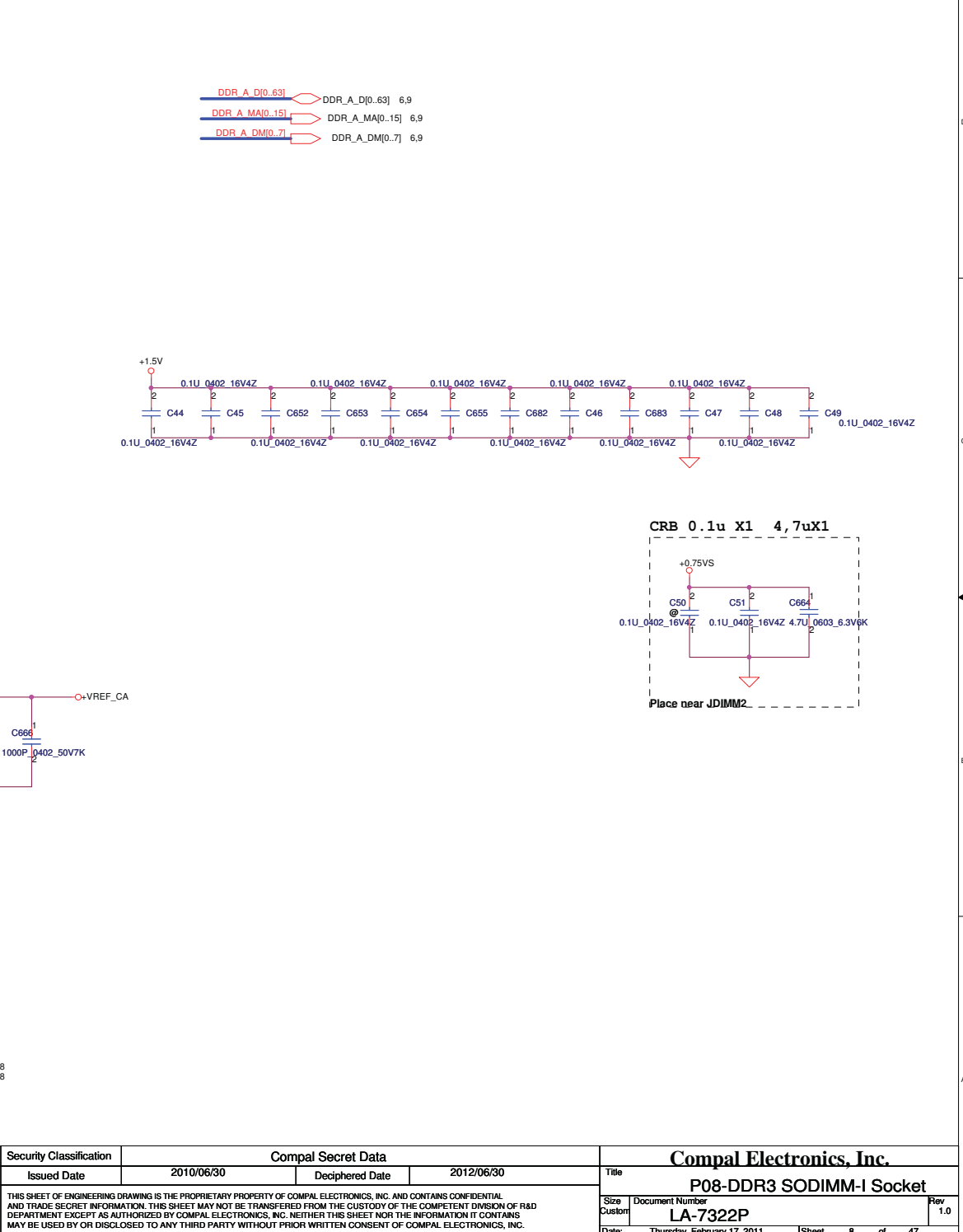
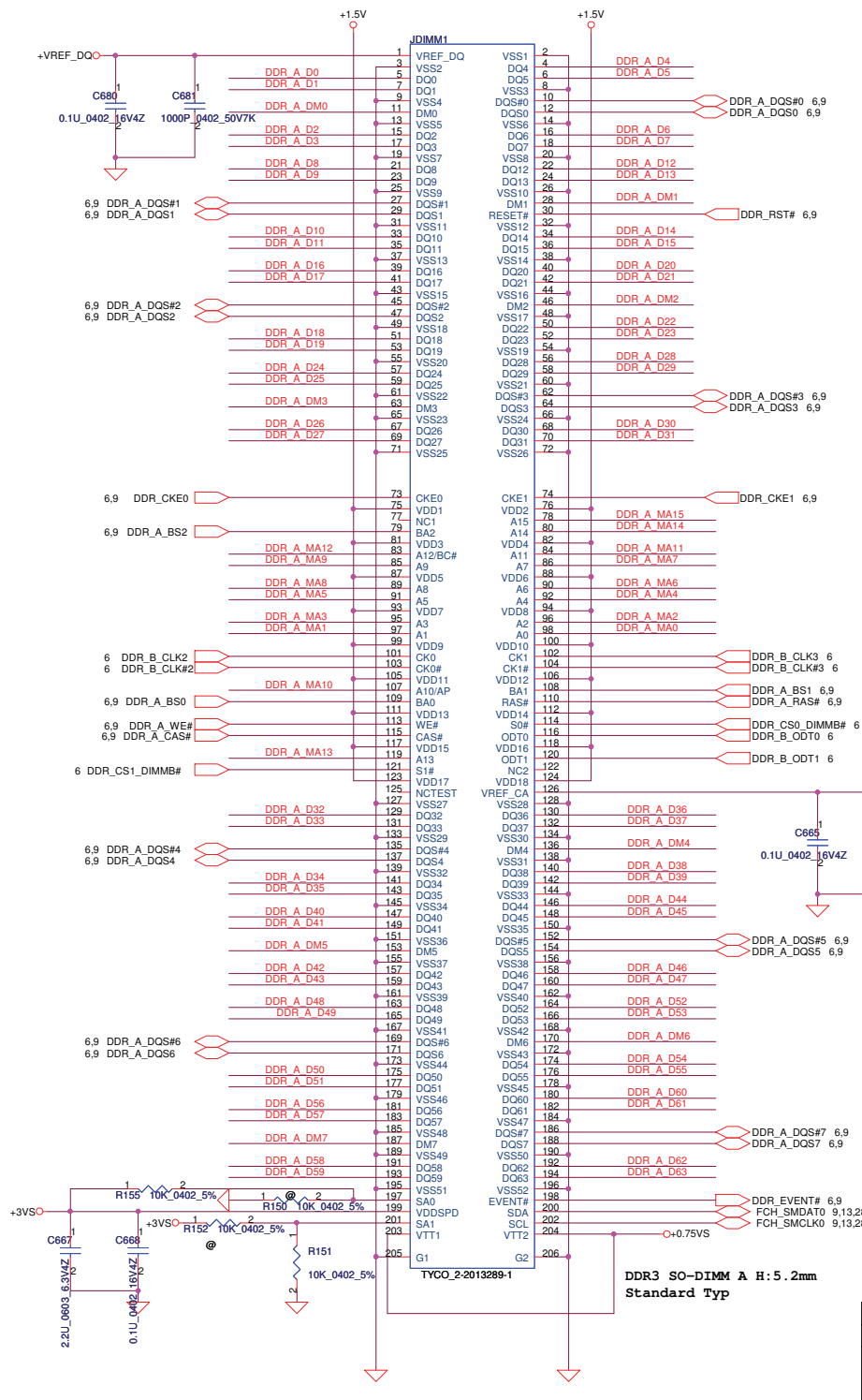
Power Cap. Summary

- APU**
- S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 ---->+APU_CORE(Qty : 3) Unpop:2
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE(Qty : 2) +APU_CORE
- S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+APU_CORE_NB(Qty : 1)
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE_NB(Qty : 1) +APU_CORE_NB
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5V(Qty : 1) +1.5V
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.05V(Qty : 1) +1.05V
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.8V(Qty : 1) +1.8V
- DDR3 Socket**
- S POLY C 330U 2V M X LESR6M SX H1.9 ---->+1.5V(Qty : 1) +1.5V
- FCH**
- S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+1.1VS(Qty : 1) UMA unpop +1.1VS
- GPU**
- S POLY C 330U 2V M X LESR6M SX H1.9 ---->+VGA_CORE(Qty : 2) Unpop:1
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+VGA_CORE(Qty : 1) +GPU_CORE
- S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5VSG(Qty : 1) +1.5VSG
- USB**
- S A-P_CAP 220U 6.3V M C45 R17M SVPE H4.4 ---->+USB_VCCA(Qty : 1) +USB_VCCA



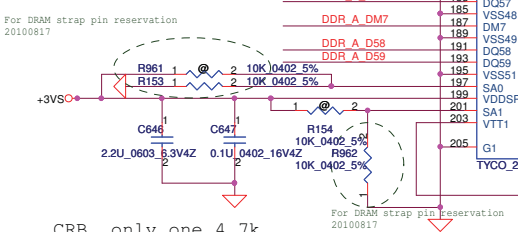
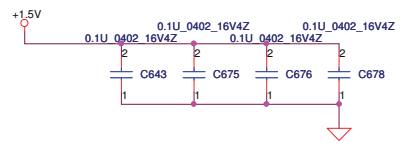
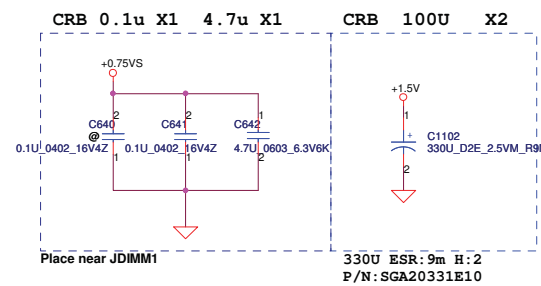
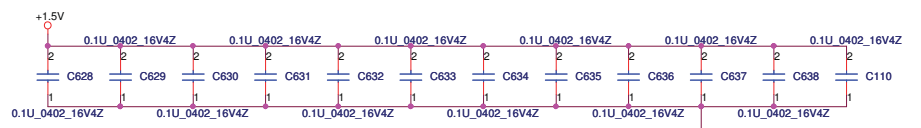
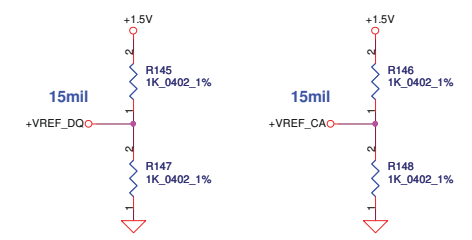
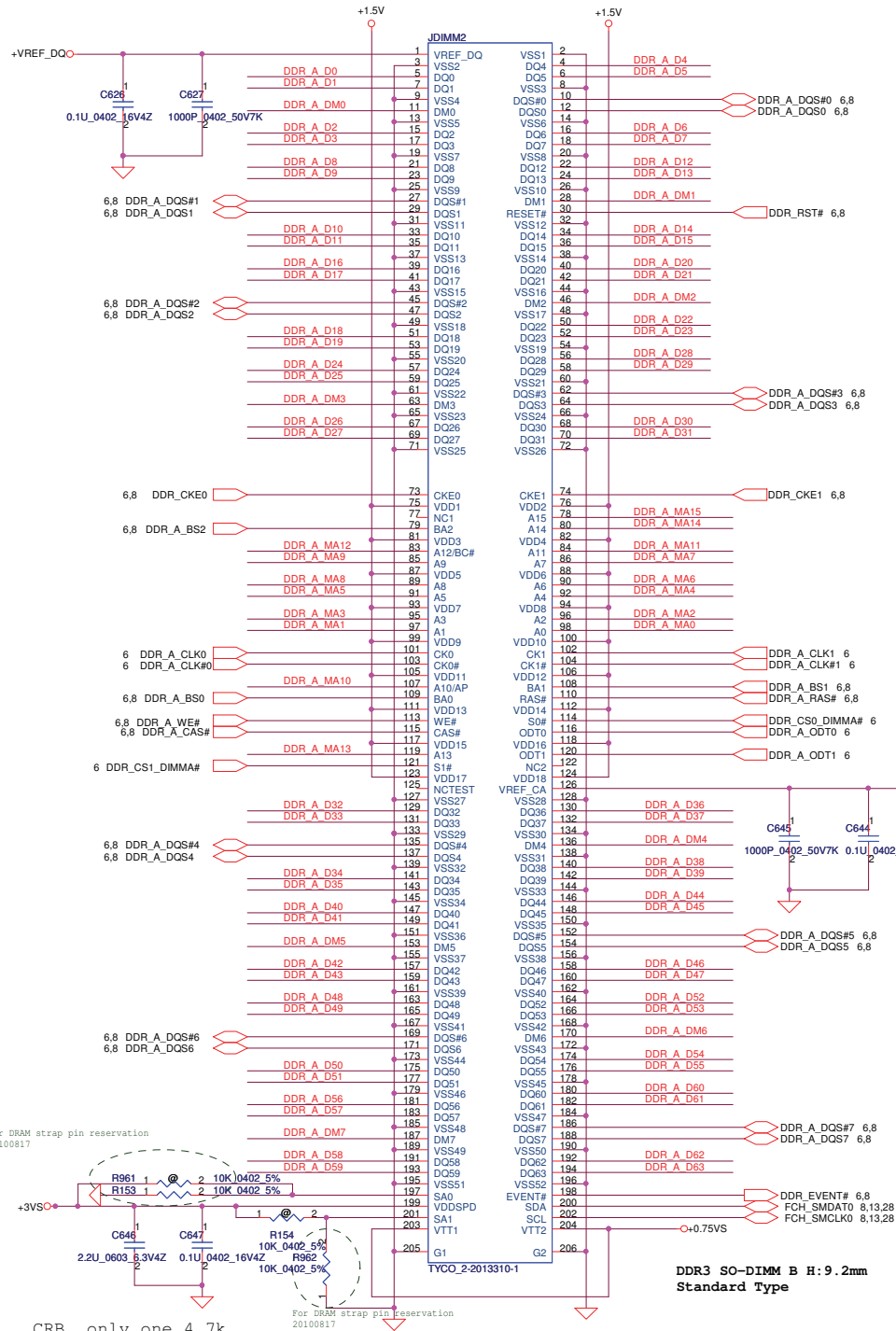
$(390\mu F \cdot 2.5V \cdot 6.3 \times 5.7 \cdot ESR10m) * 1 = (SF000002000)$





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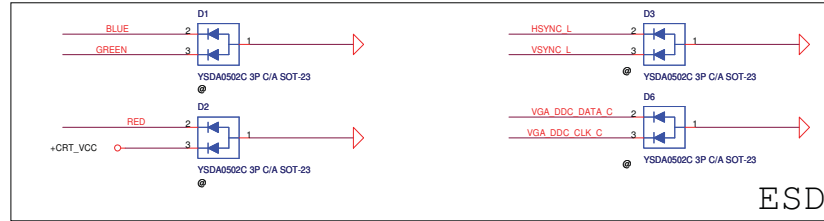
Compal Electronics, Inc.			
Title P08-DDR3 SODIMM-I Socket			
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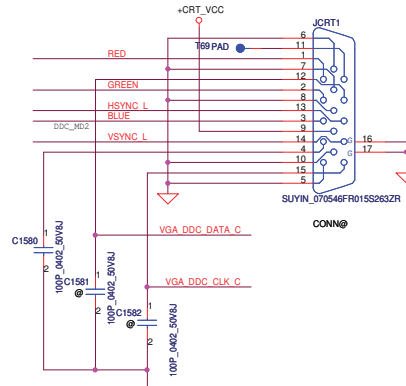
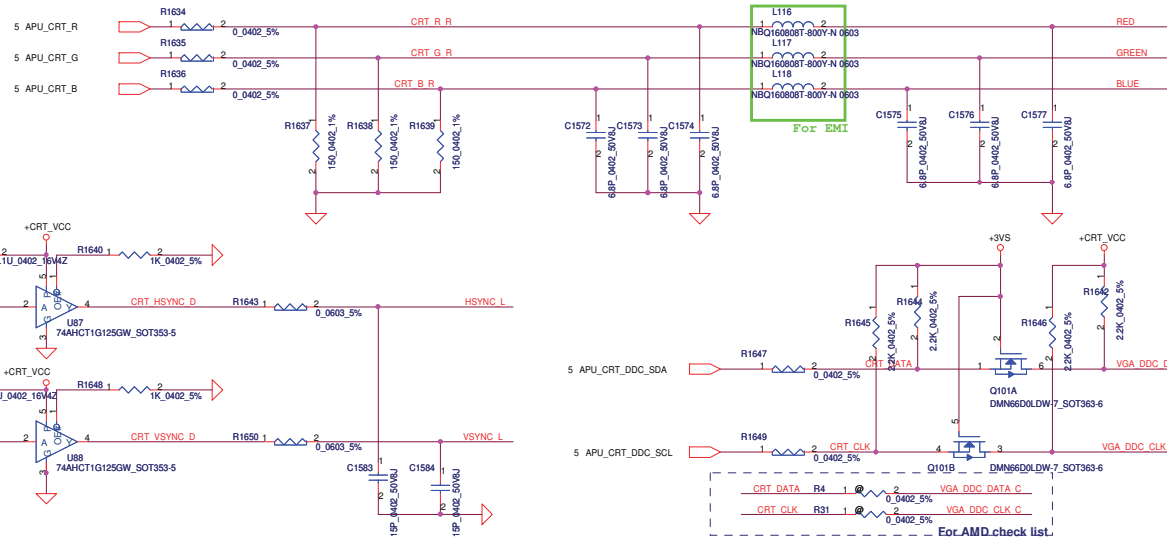
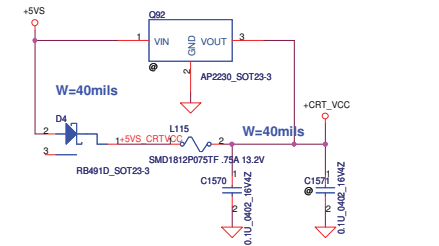
DDR3 SO-DIMM B H:9.2mm
Standard Type

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				Document Number	1.0
				LA-7322P	
				Date:	Thursday, February 17, 2011
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CRT



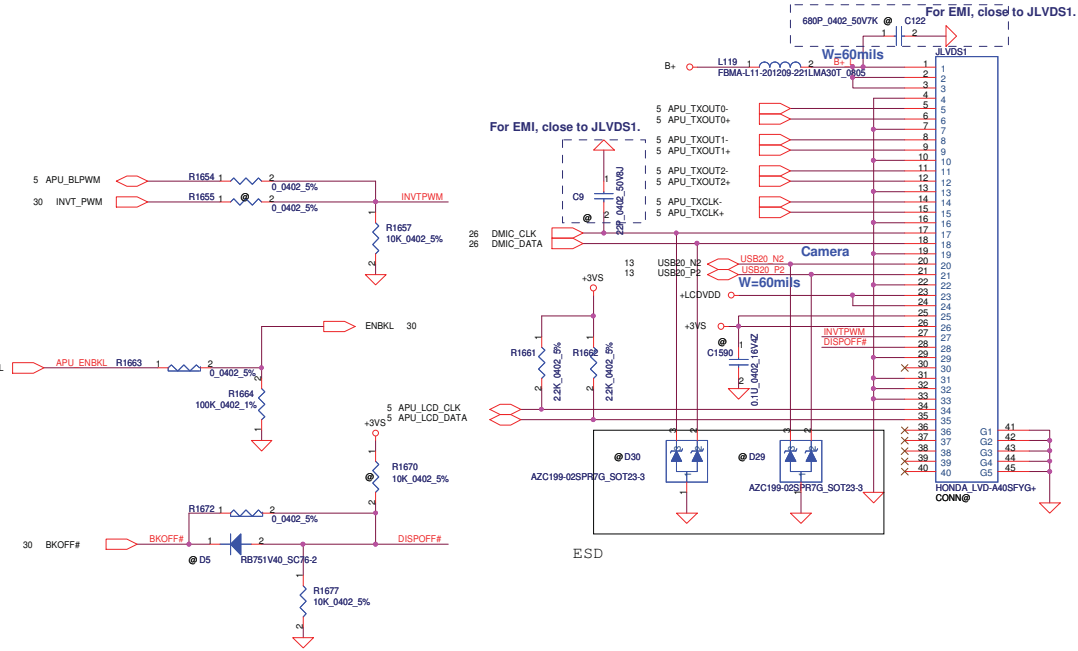
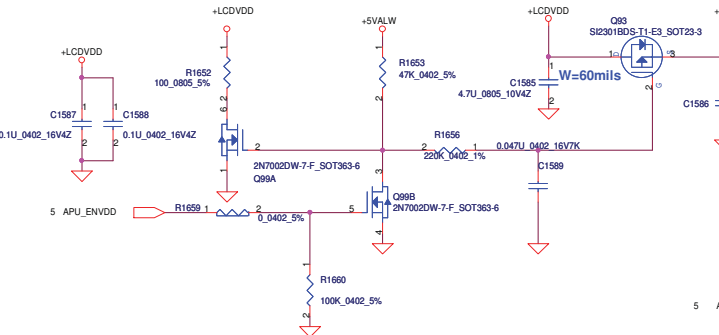
ESD



Close to APU

For AMD check list

LCD POWER CIRCUIT



For EMI, close to JLVDS1.

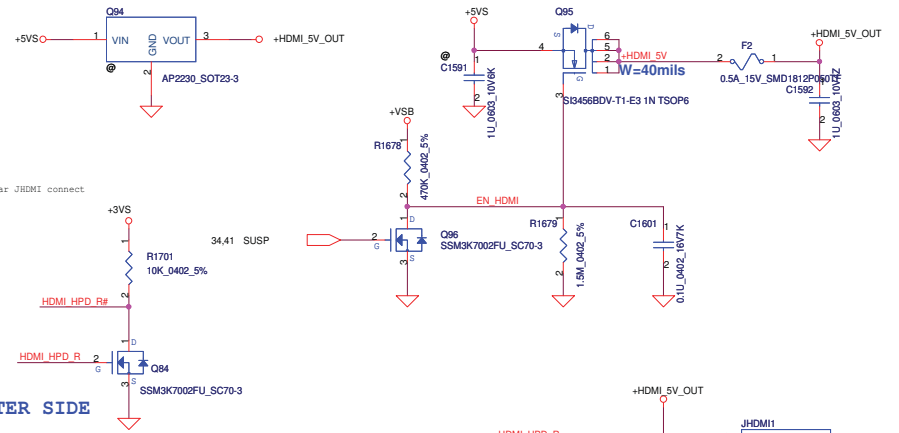
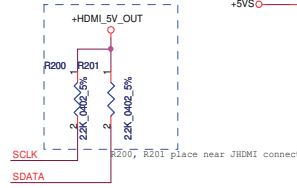
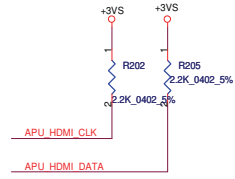
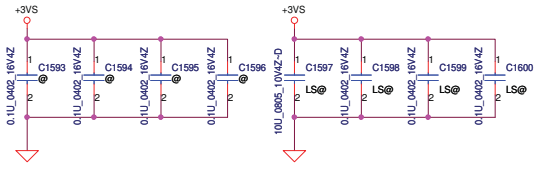
For EMI, close to JLVDS1.

Camera

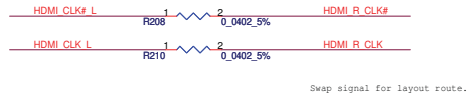
ESD

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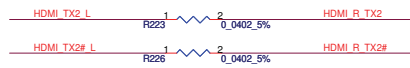
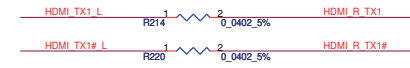
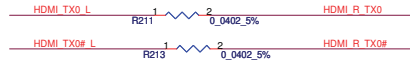
close to U10VCC (+3VS) pins (one Pin one Capacitor)



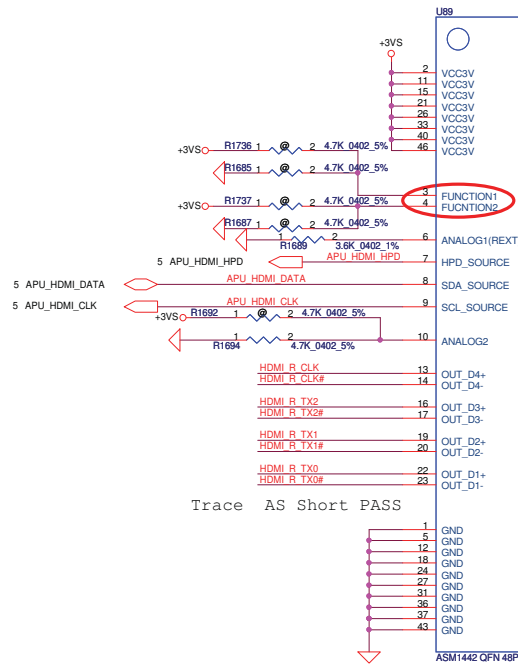
5 APU_HDMI_CLKP	C1602	1	2	0.1U 0402 16V7K	HDMI_CLK
5 APU_HDMI_CLKN	C1603	1	2	0.1U 0402 16V7K	HDMI_CLK#
5 APU_HDMI_TX0P	C1604	1	2	0.1U 0402 16V7K	HDMI_TX0
5 APU_HDMI_TX0N	C1605	1	2	0.1U 0402 16V7K	HDMI_TX0#
5 APU_HDMI_TX1P	C1606	1	2	0.1U 0402 16V7K	HDMI_TX1
5 APU_HDMI_TX1N	C1607	1	2	0.1U 0402 16V7K	HDMI_TX1#
5 APU_HDMI_TX2P	C1608	1	2	0.1U 0402 16V7K	HDMI_TX2
5 APU_HDMI_TX2N	C1609	1	2	0.1U 0402 16V7K	HDMI_TX2#



Swap signal for layout route.

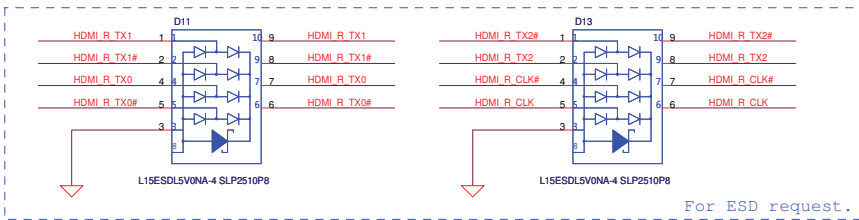
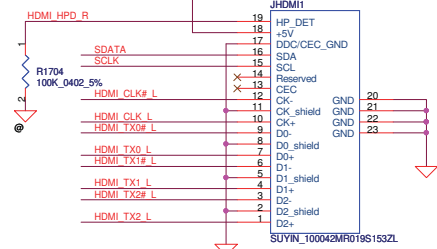
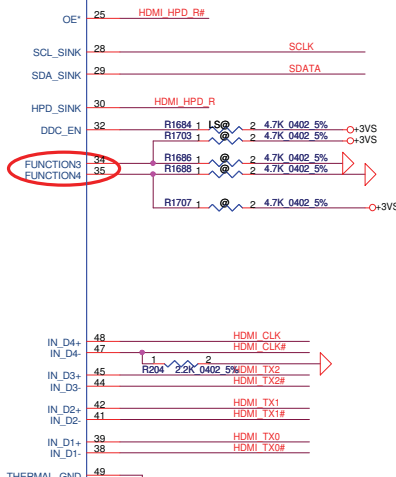


5V PULL UP IN CONNECTER SIDE

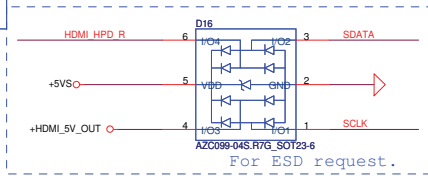


Trace AS Short PASS

ASM1442 OFN 48P

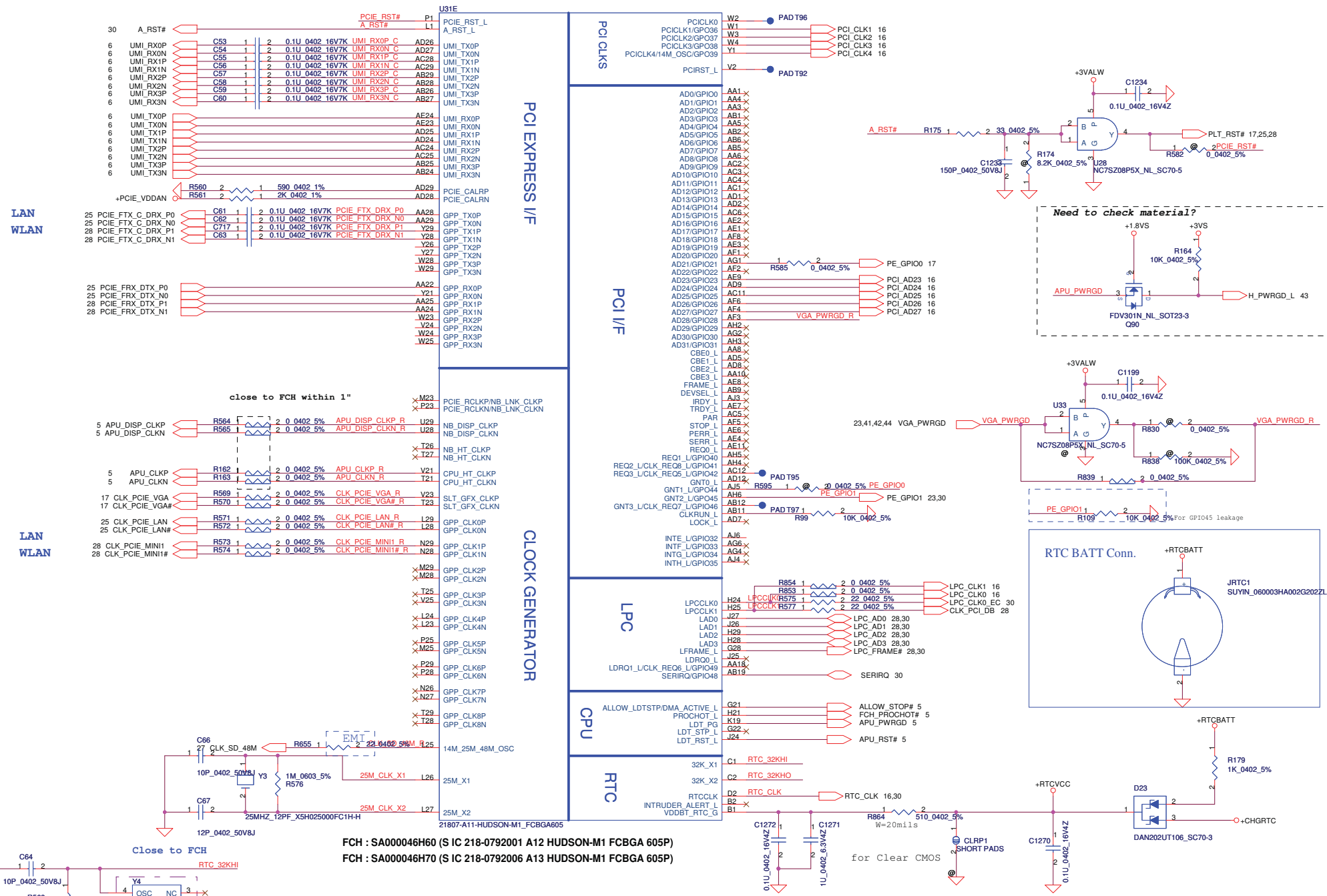


For ESD request.



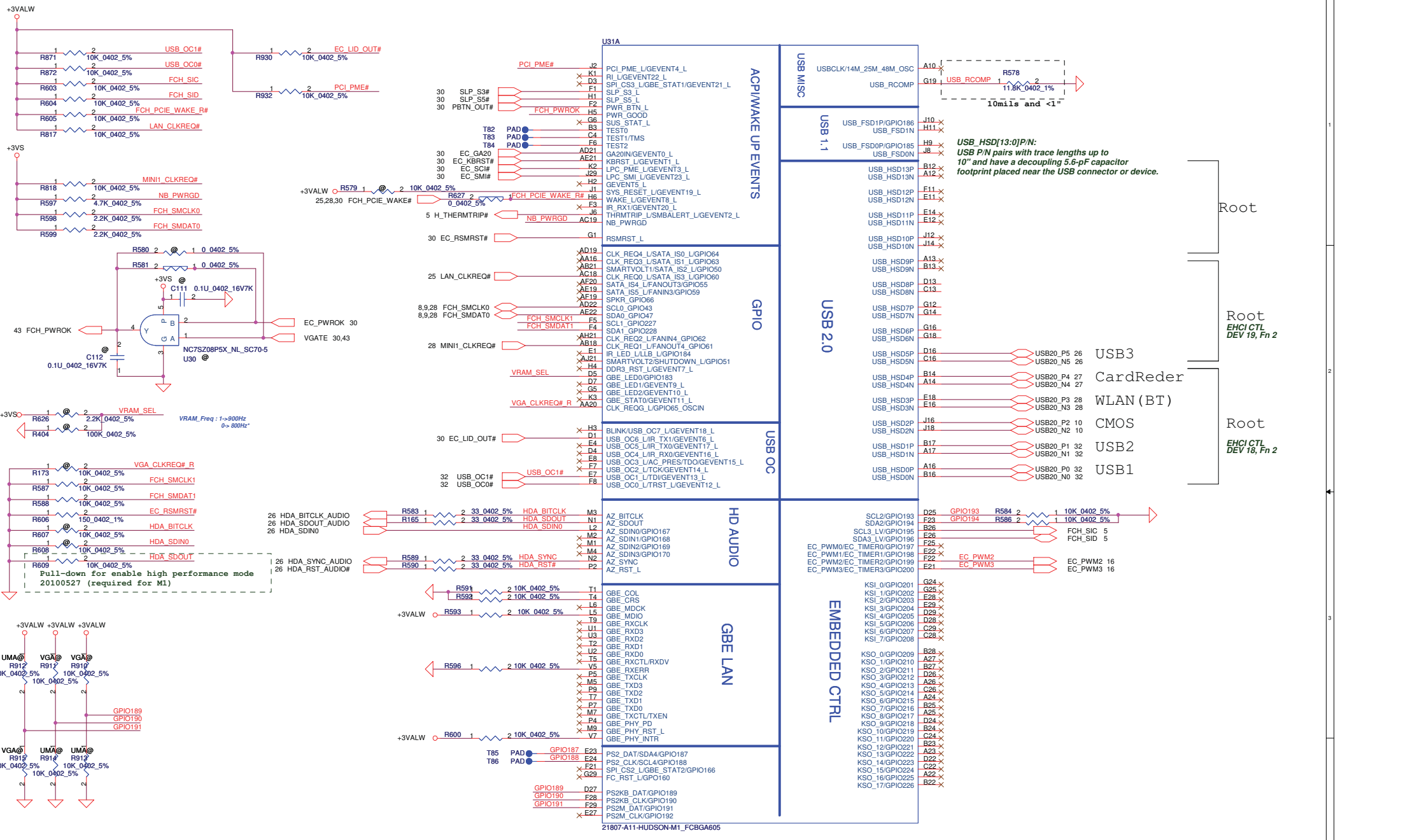
For ESD request.

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				P11-HDMI CONN
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FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)
 FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	P12-FCH PCIE/PCI/ACPI/LPC/RTC	
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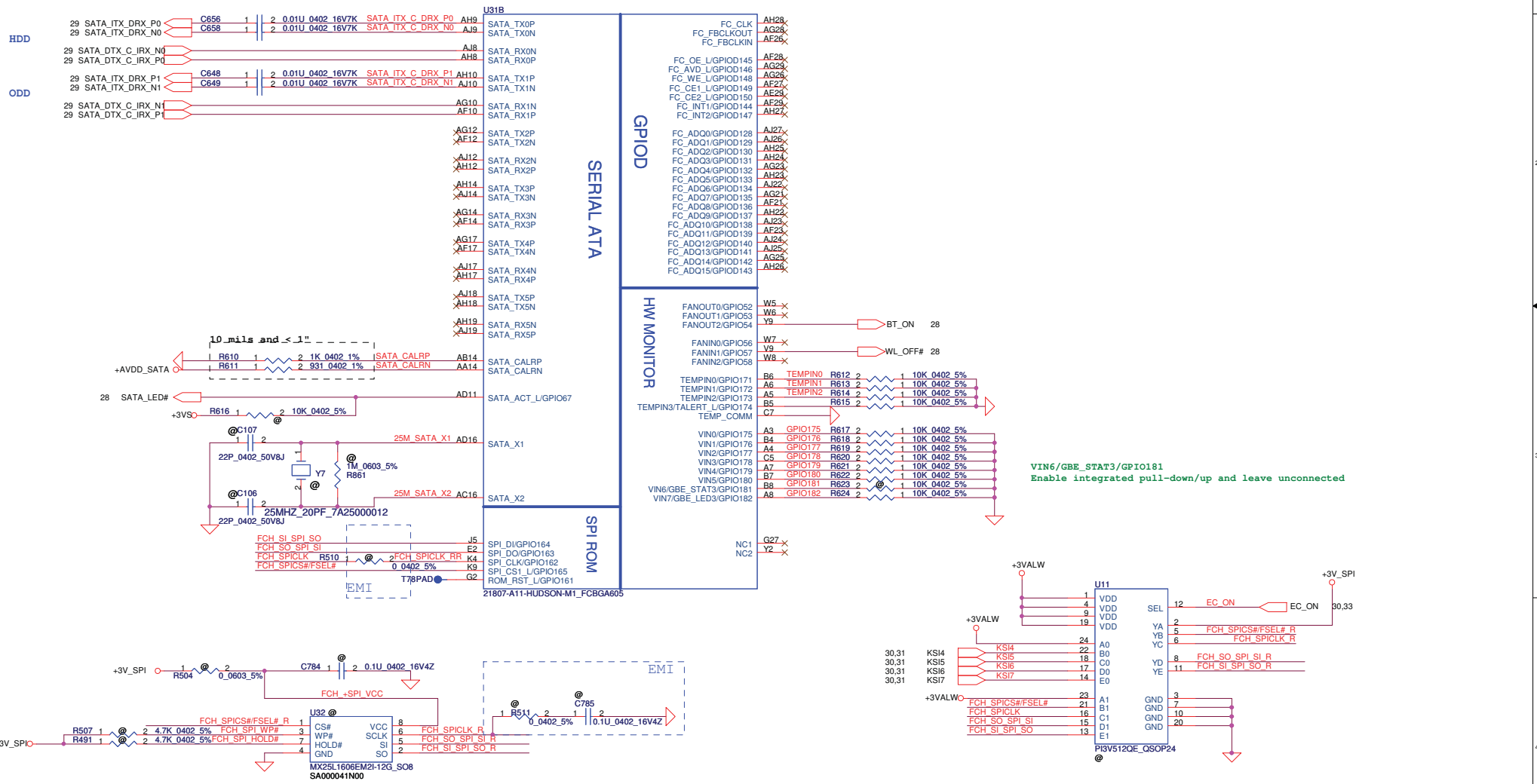
SKU_ID (GPIO189)	SKU_ID : 1->VGA* 0->UMA
PX_FN (GPIO190)	PX_Function : 1->PX Enable* 0->PX Disable
PX_SEL (GPIO191)	PX_SEL : 1->PX 3.0* 0->PX 4.0

GPIO	189	190	191
UMA	0	0	1
DISO	1	0	1
PX3.0	1	1	1
PX4.0	1	1	0

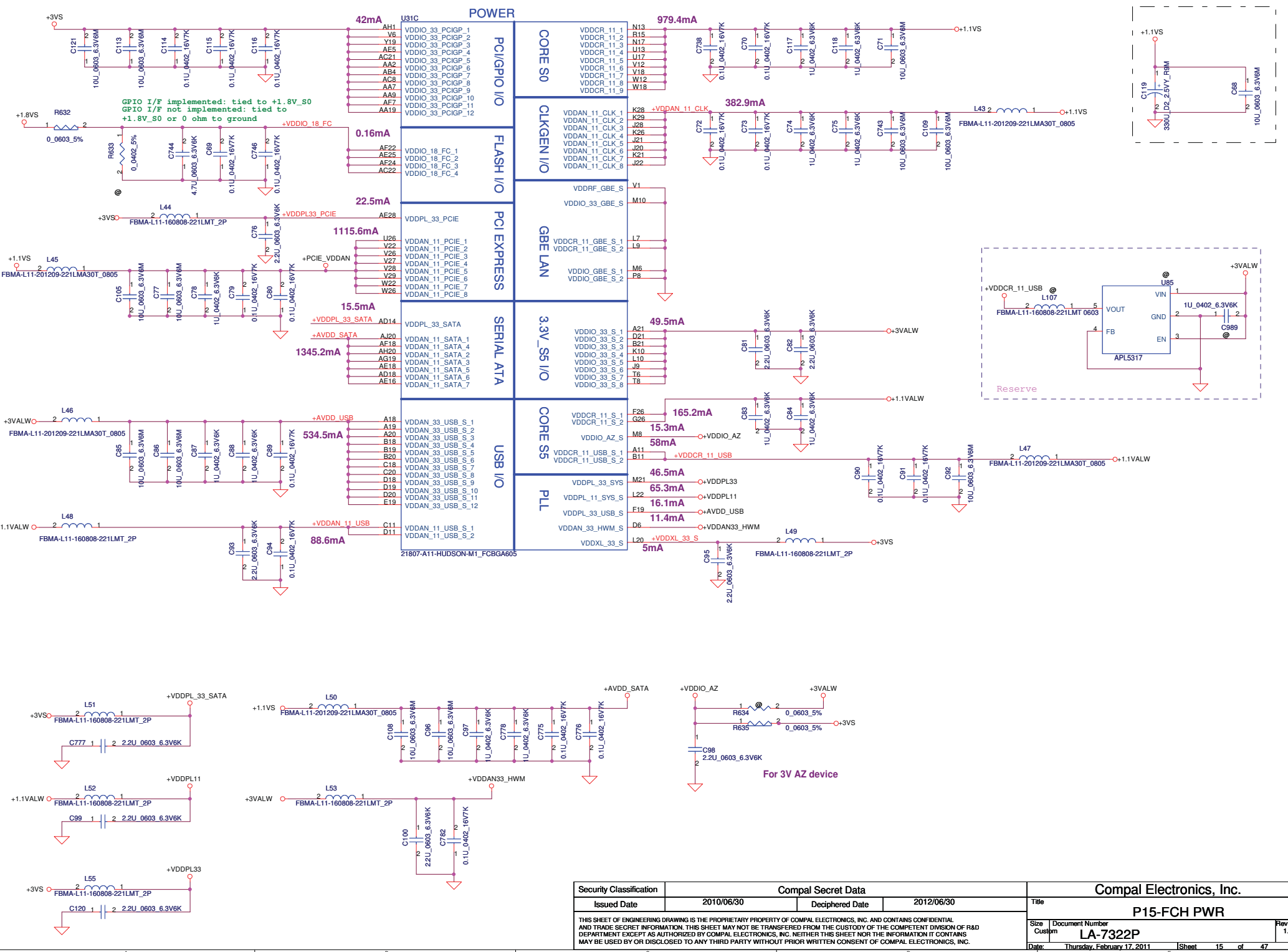
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Issued Date	2010/06/30	Deciphered Date
		2012/06/30

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Title		
P13-FCH HDA/USB/ACPI		
Size	Document Number	Rev
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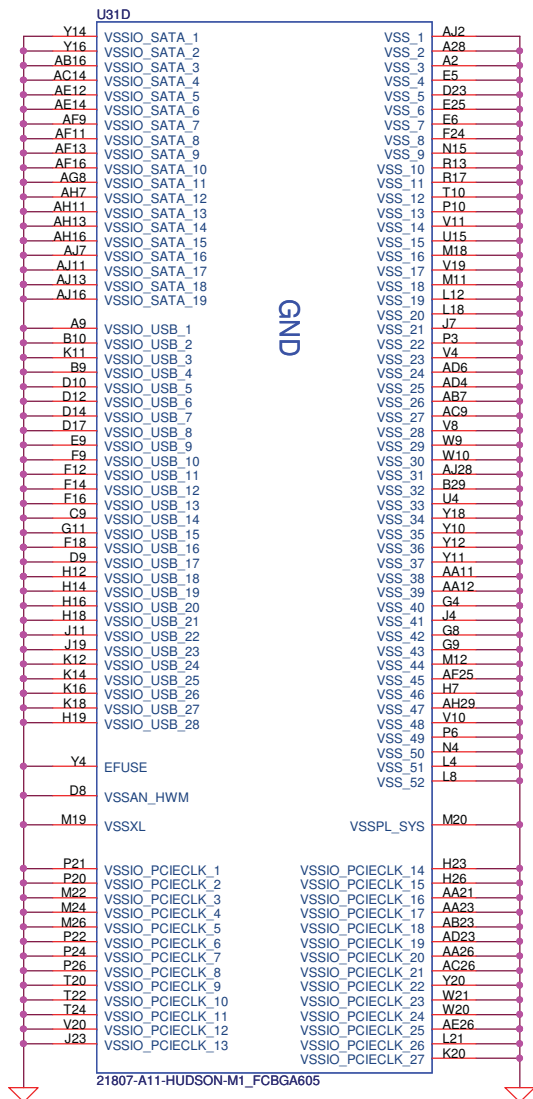


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				P14-FCH-SATA/SPI		
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Compal Electronics, Inc.			
Title			
P15-FCH PWR			
Size	Document Number	Rev	
Custom	LA-7322P	1.0	
Date:	Thursday, February 17, 2011	Sheet	15 of 47

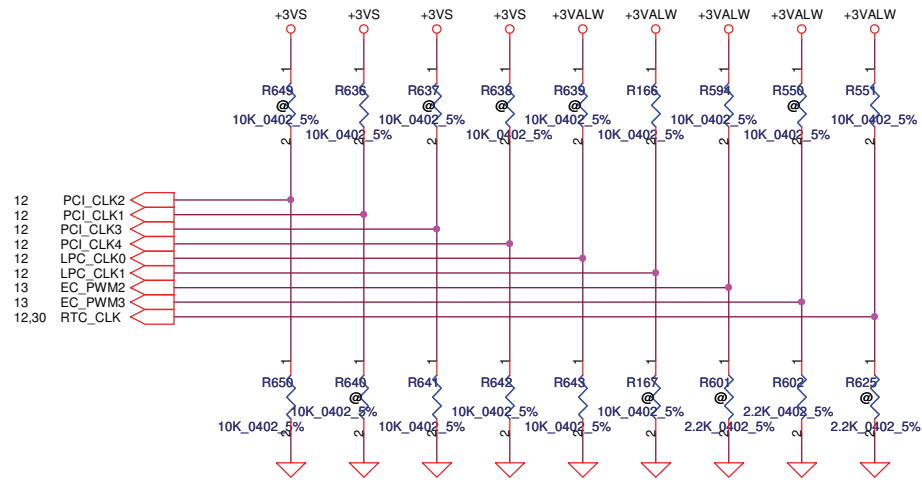


21807-A11-HUDSON-M1_FCBGA605

REQUIRED STRAPS

Check Internal PU/PD

PULL HIGH	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L)
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)

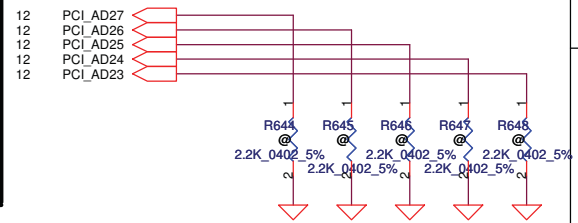


DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

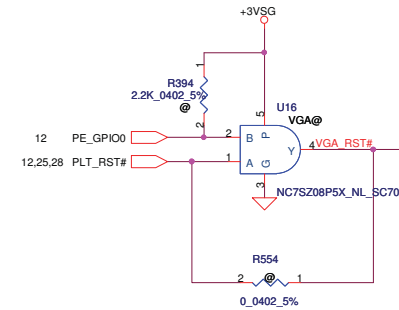
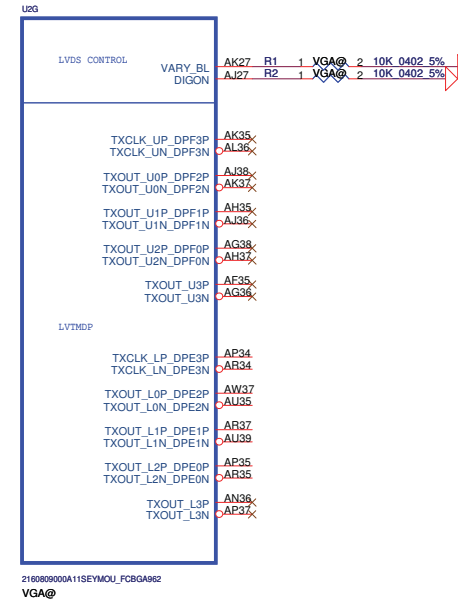
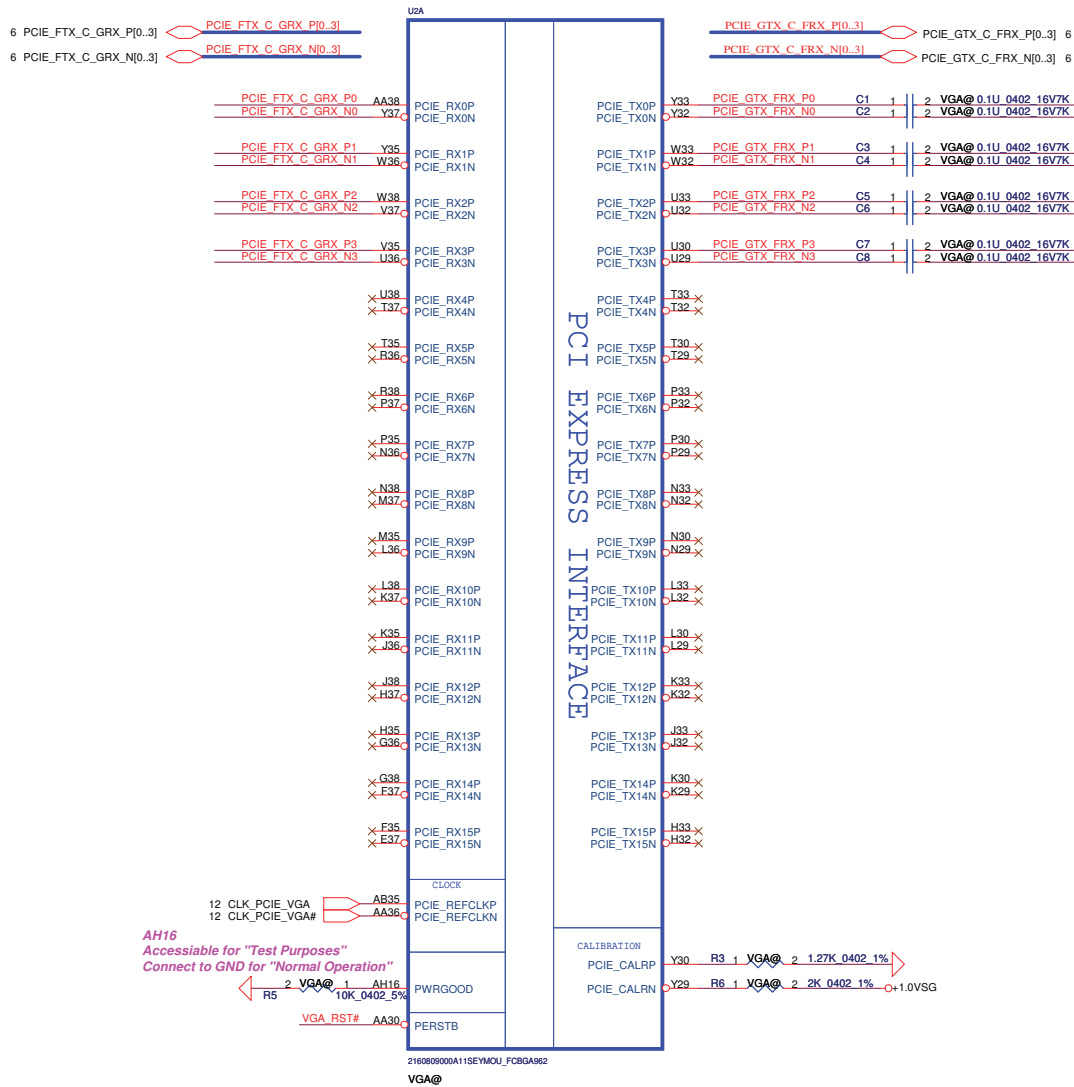
PULL HIGH	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function check default



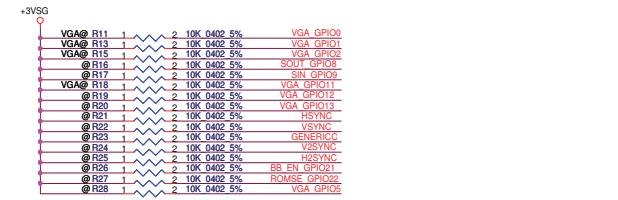
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title P16-FCH-VSS/Strap		
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GFX PCIE LANE REVERSAL

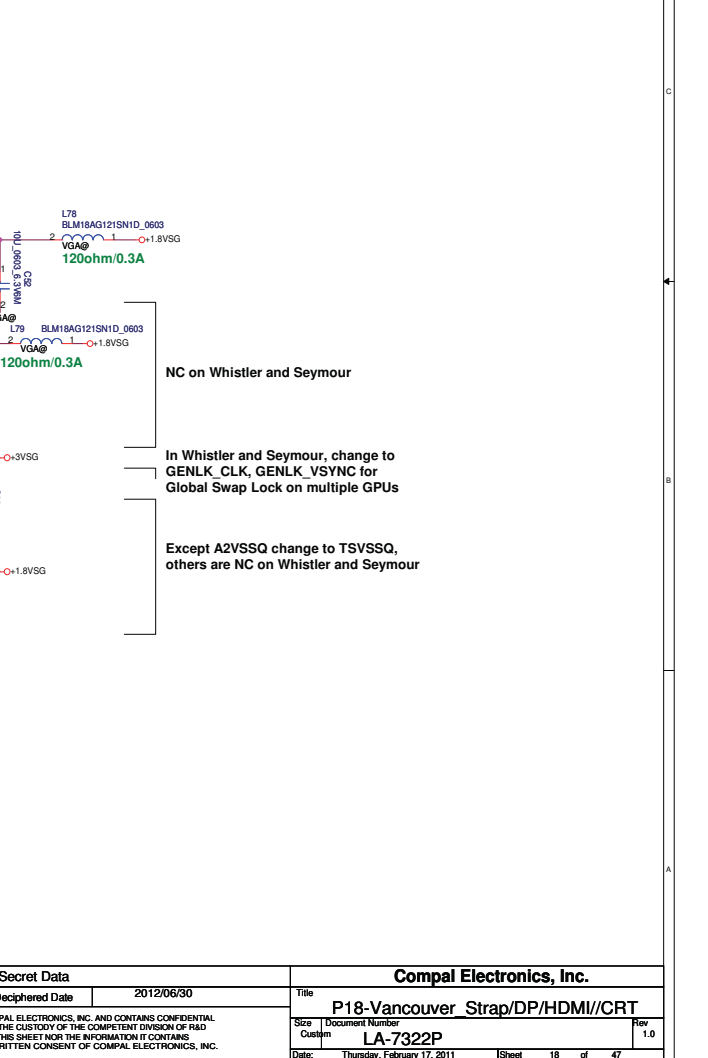
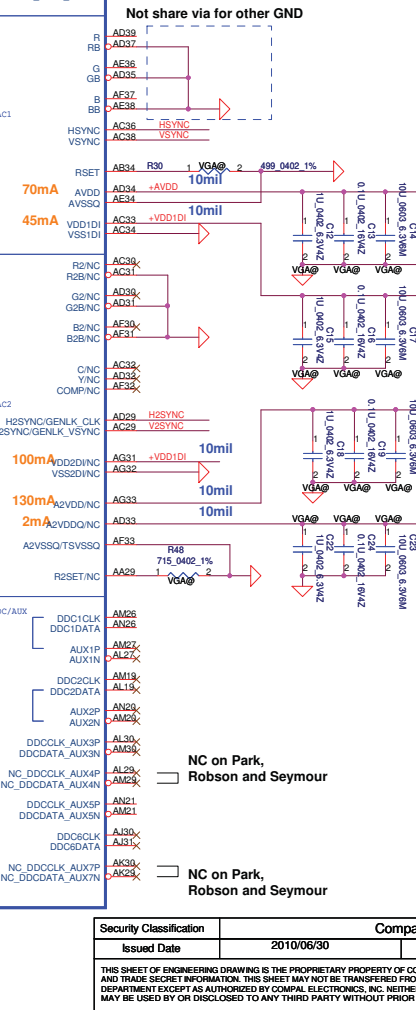
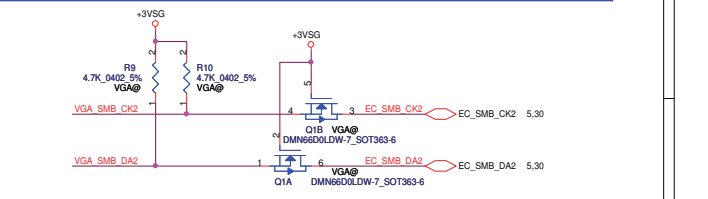
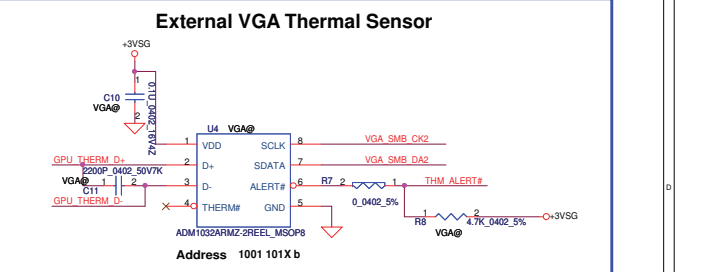
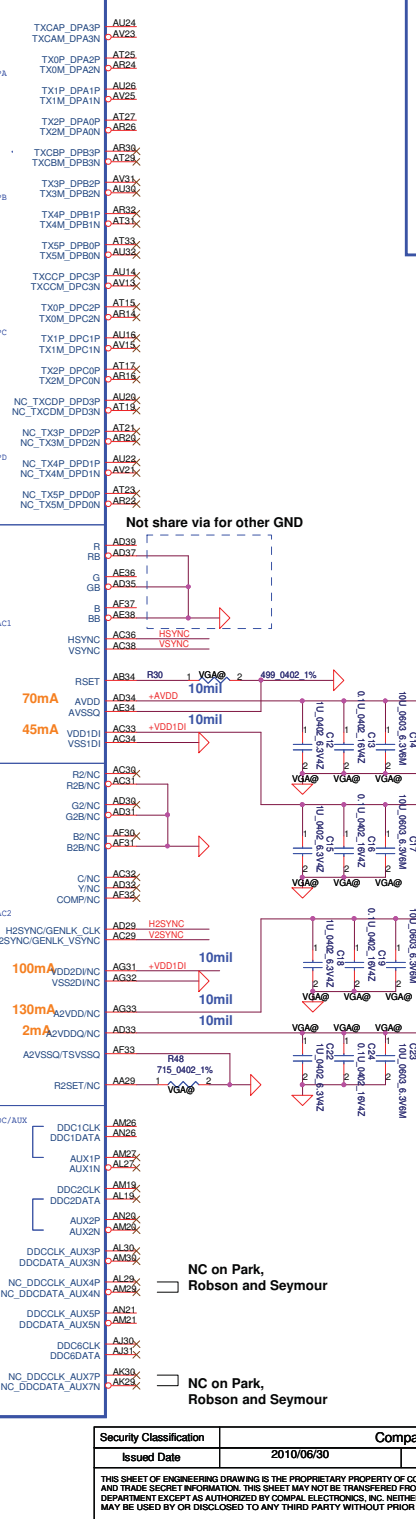
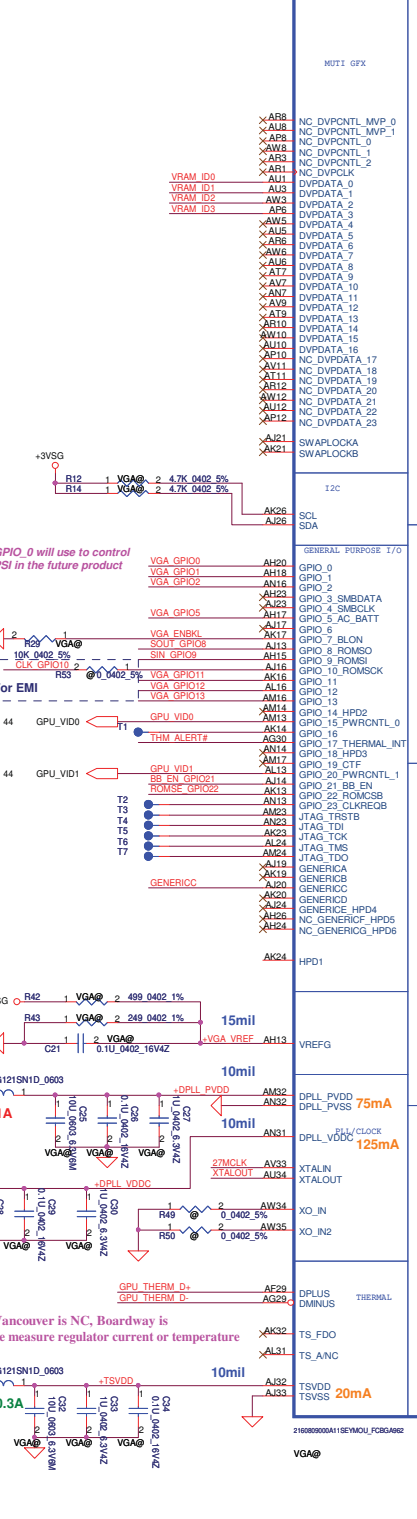
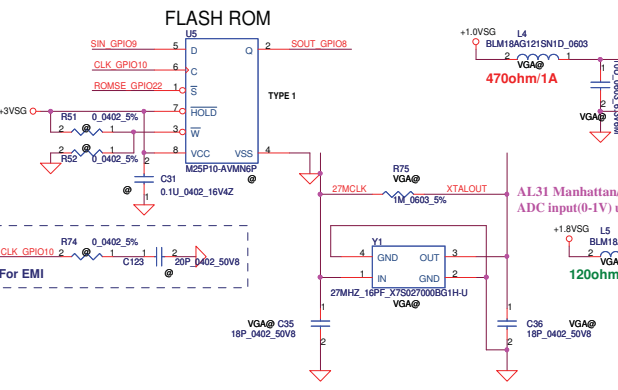
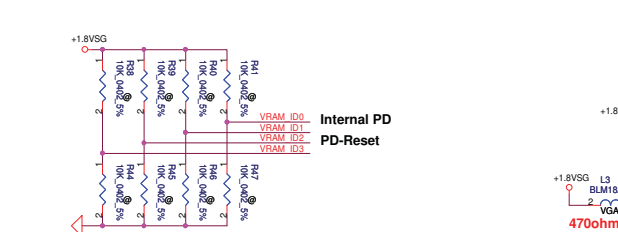


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				P17-Vancouver_PCIE / LVDS	
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Strap Name	Pin Straps description <-all internal PD->	Setting
VGA_DIS	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM type. memory apertures 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	0= Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

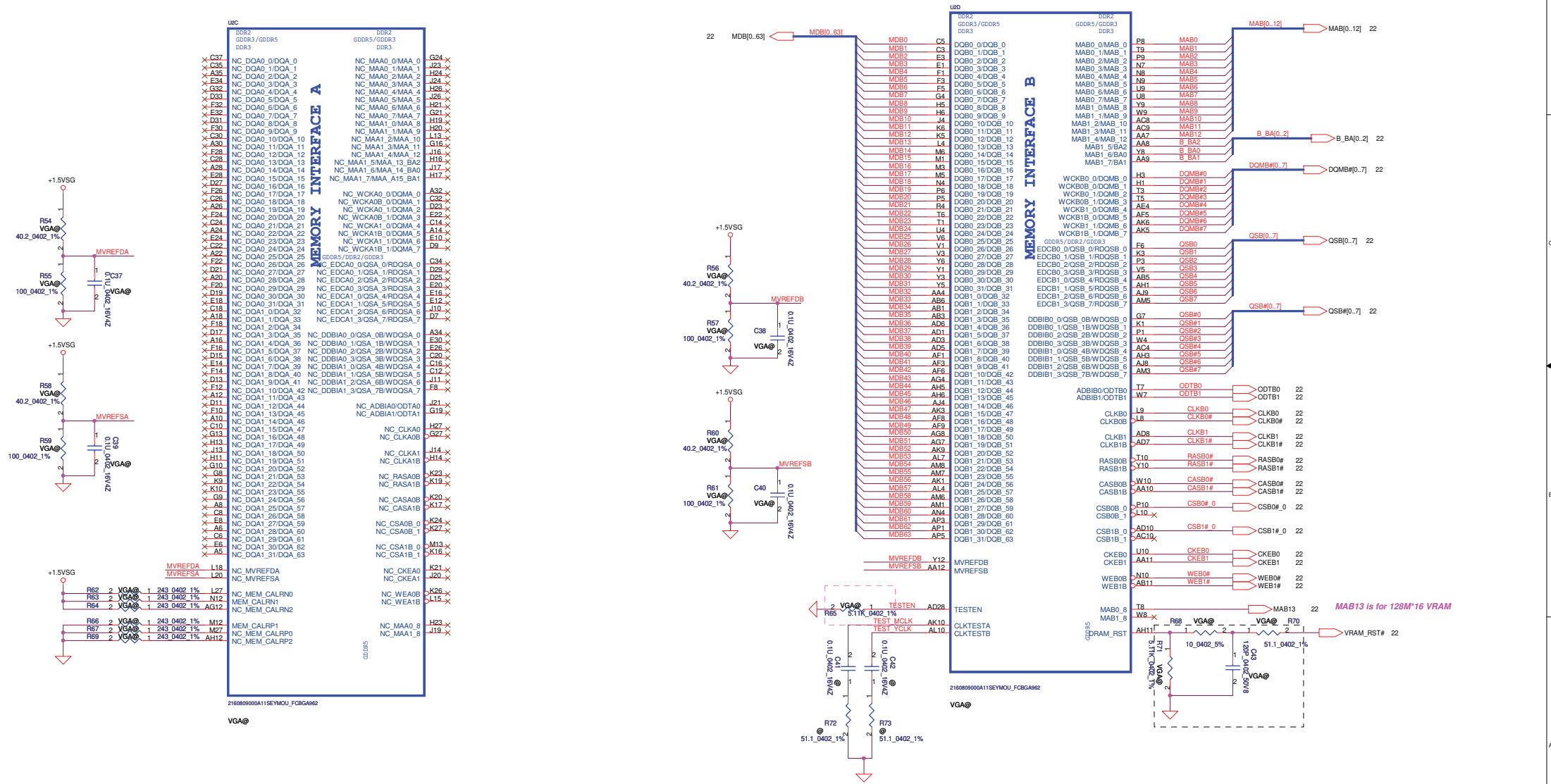


VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004GS30	64M16	0	0	0	0
Samsung SA00004GS40	128M16	0	0	0	1
Samsung SA00004S60	64M16	0	1	0	0
Hynix SA00003Y030	128M16	0	1	0	1



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				Sheet	18 of 47

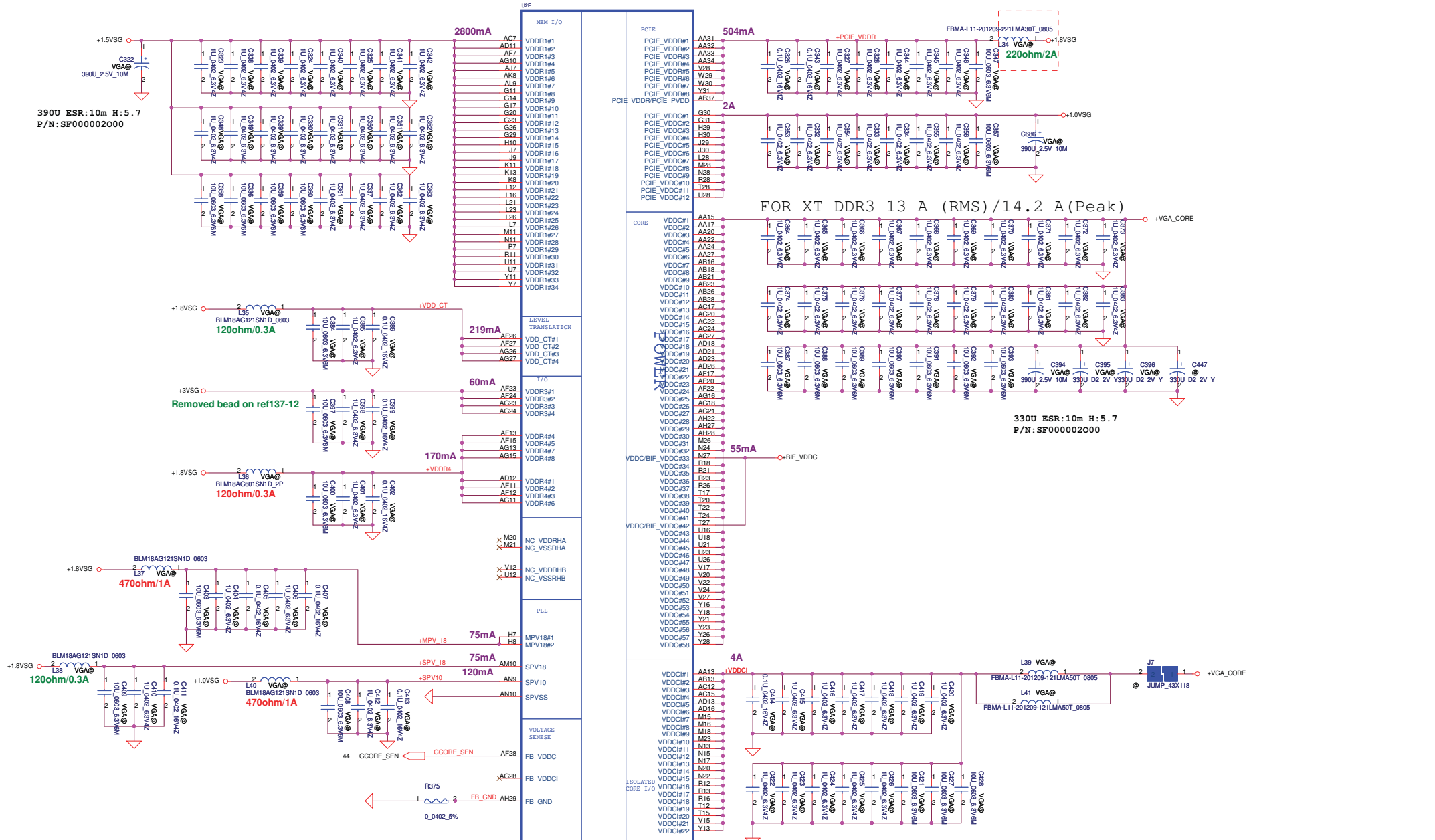
Robson, Seymour only support single channel memory (channel B only)



MEMORY INTERFACE A

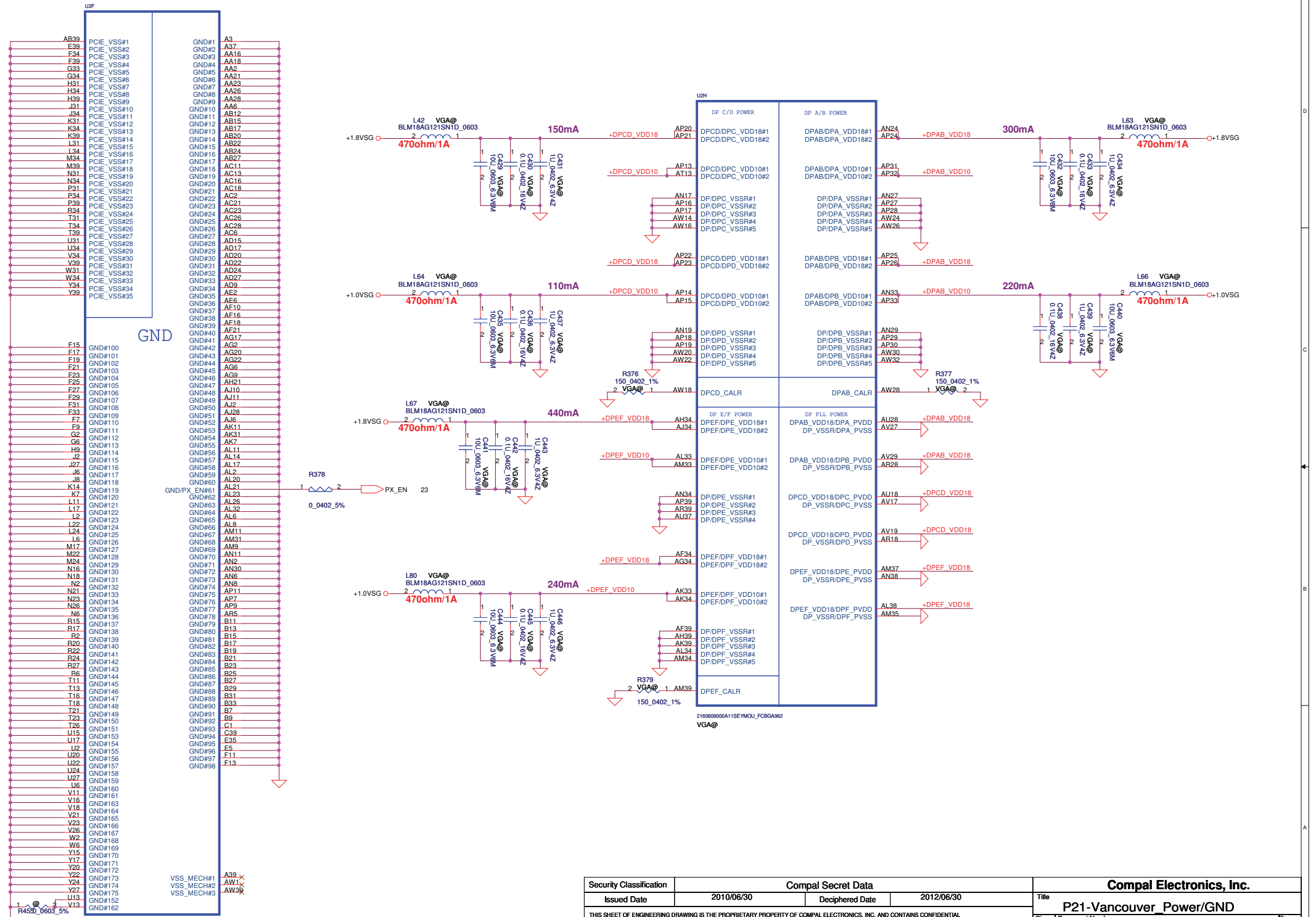
DDR2 GDDR3/GDDR5 DDR3	DDR2 GDDR3/GDDR5 DDR3	DDR2 GDDR3/GDDR5 DDR3
X37	NC_DDA0_0/DDA_0	NC_MAA0_0/MAA_0
X38	NC_DDA0_1/DDA_1	NC_MAA0_1/MAA_1
A35	NC_DDA0_2/DDA_2	NC_MAA0_2/MAA_2
X34	NC_DDA0_3/DDA_3	NC_MAA0_3/MAA_3
X33	NC_DDA0_4/DDA_4	NC_MAA0_4/MAA_4
D33	NC_DDA0_5/DDA_5	NC_MAA0_5/MAA_5
F32	NC_DDA0_6/DDA_6	NC_MAA0_6/MAA_6
X32	NC_DDA0_7/DDA_7	NC_MAA0_7/MAA_7
D31	NC_DDA0_8/DDA_8	NC_MAA1_0/MAA_8
F30	NC_DDA0_9/DDA_9	NC_MAA1_1/MAA_9
X30	NC_DDA0_10/DDA_10	NC_MAA1_2/MAA_10
X31	NC_DDA0_11/DDA_11	NC_MAA1_3/MAA_11
F29	NC_DDA0_12/DDA_12	NC_MAA1_4/MAA_12
X28	NC_DDA0_13/DDA_13	NC_MAA1_5/MAA_13_BA2
A28	NC_DDA0_14/DDA_14	NC_MAA1_6/MAA_14_BA0
E28	NC_DDA0_15/DDA_15	NC_MAA1_7/MAA_15_BA1
D27	NC_DDA0_16/DDA_16	
F26	NC_DDA0_17/DDA_17	NC_WCKA0_0/DOMA_0
X26	NC_DDA0_18/DDA_18	NC_WCKA0_1/DOMA_1
A26	NC_DDA0_19/DDA_19	NC_WCKA0_2/DOMA_2
X24	NC_DDA0_20/DDA_20	NC_WCKA0B_1/DOMA_3
X23	NC_DDA0_21/DDA_21	NC_WCKA1_0/DOMA_4
A24	NC_DDA0_22/DDA_22	NC_WCKA1B_0/DOMA_5
E24	NC_DDA0_23/DDA_23	NC_WCKA1_1/DOMA_6
D22	NC_DDA0_24/DDA_24	NC_WCKA1B_1/DOMA_7
F22	NC_DDA0_25/DDA_25	NC_WCKA1B_2/DOMA_8
X22	NC_DDA0_26/DDA_26	NC_EDCA0_0/OSA_0/RDOSA_0
A20	NC_DDA0_27/DDA_27	NC_EDCA0_1/OSA_1/RDOSA_1
X20	NC_DDA0_28/DDA_28	NC_EDCA0_2/OSA_2/RDOSA_2
F20	NC_DDA0_29/DDA_29	NC_EDCA0_3/OSA_3/RDOSA_3
X19	NC_DDA0_30/DDA_30	NC_EDCA0_4/OSA_4/RDOSA_4
D18	NC_DDA0_31/DDA_31	NC_EDCA1_0/OSA_5/RDOSA_5
E18	NC_DDA0_32/DDA_32	NC_EDCA1_1/OSA_6/RDOSA_6
X18	NC_DDA0_33/DDA_33	NC_EDCA1_2/OSA_7/RDOSA_7
F18	NC_DDA1_2/DDA_34	NC_DDBIA0_0/OSA_0B/WDOSA_0
X16	NC_DDA1_3/DDA_35	NC_DDBIA0_1/OSA_1B/WDOSA_1
A16	NC_DDA1_4/DDA_36	NC_DDBIA0_2/OSA_2B/WDOSA_2
X15	NC_DDA1_5/DDA_37	NC_DDBIA0_3/OSA_3B/WDOSA_3
D15	NC_DDA1_6/DDA_38	NC_DDBIA0_4/OSA_4B/WDOSA_4
E14	NC_DDA1_7/DDA_39	NC_DDBIA1_0/OSA_4B/WDOSA_4
X14	NC_DDA1_8/DDA_40	NC_DDBIA1_1/OSA_5B/WDOSA_5
F14	NC_DDA1_9/DDA_41	NC_DDBIA1_2/OSA_6B/WDOSA_6
X13	NC_DDA1_10/DDA_42	NC_DDBIA1_3/OSA_7B/WDOSA_7
D13	NC_DDA1_11/DDA_43	
E12	NC_DDA1_12/DDA_44	NC_ADBIA0/ODTA0
X12	NC_DDA1_13/DDA_45	NC_ADBIA1/ODTA1
A10	NC_DDA1_14/DDA_46	
X10	NC_DDA1_15/DDA_47	NC_CLKA0
F10	NC_DDA1_16/DDA_48	NC_CLKA0B
X9	NC_DDA1_17/DDA_49	
D9	NC_DDA1_18/DDA_50	NC_CLKA1
E9	NC_DDA1_19/DDA_51	NC_CLKA1B
X8	NC_DDA1_20/DDA_52	
F8	NC_DDA1_21/DDA_53	NC_RASA0B
X7	NC_DDA1_22/DDA_54	NC_RASA1B
D7	NC_DDA1_23/DDA_55	
E7	NC_DDA1_24/DDA_56	NC_CASA0B
X6	NC_DDA1_25/DDA_57	NC_CASA1B
F6	NC_DDA1_26/DDA_58	
X5	NC_DDA1_27/DDA_59	NC_CSA0B_0
D5	NC_DDA1_28/DDA_60	NC_CSA0B_1
E5	NC_DDA1_29/DDA_61	NC_CSA1B_0
X4	NC_DDA1_30/DDA_62	NC_CSA1B_1
F4	NC_DDA1_31/DDA_63	

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Issued Date	2010/06/30	Deciphered Date	2012/06/30	P19-Vancouver_Memory	
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Scale	Customer	Docu	Number	Rev	
			LA-7322P	.0	
Date	Thursday, February 17, 2011	Sheet	19	of 47	



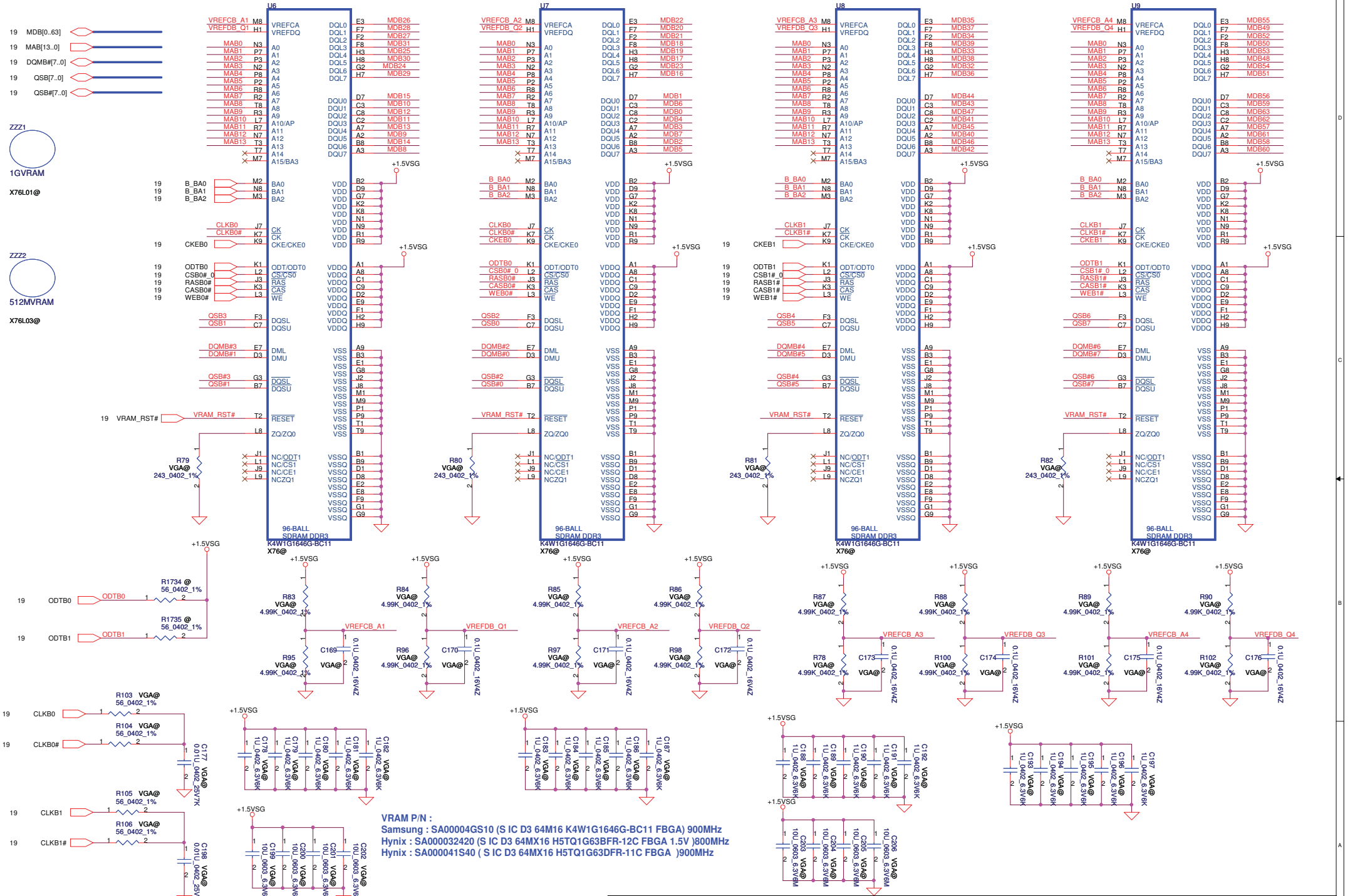
216080000A11SEVMOU_FCBG462
VGA@

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	P20-Vancouver Power/GND
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				Rev	1.0
				Date	Thursday, February 17, 2011
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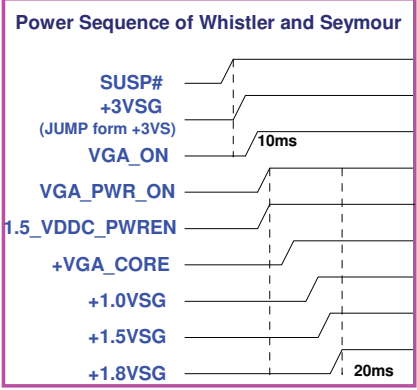
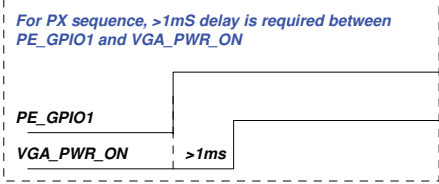
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30
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Title	P21-Vancouver Power/GND		
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VRAM P/N :
 Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA) 900MHz
 Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)900MHz
 Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA)900MHz

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				P22-VRAM DDR3 / Channel B	
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				Date: Thursday, February 17, 2011	Rev 1.0
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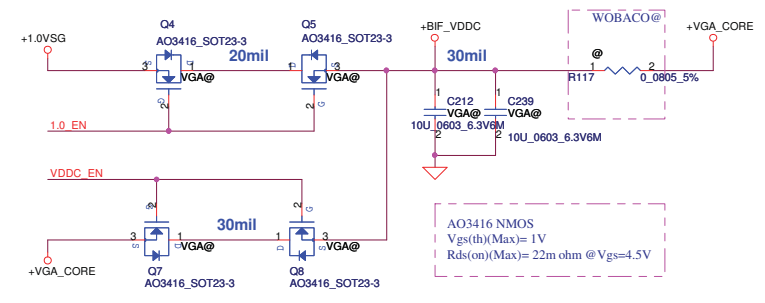
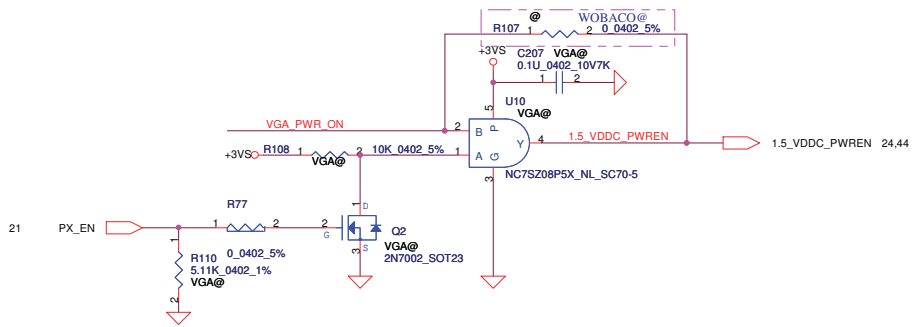
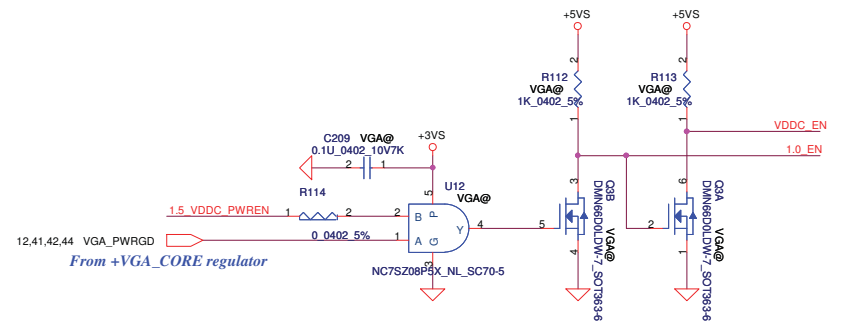
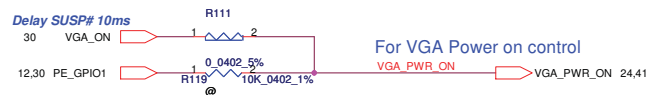


VGA Muxless with BACO Status Mapping table

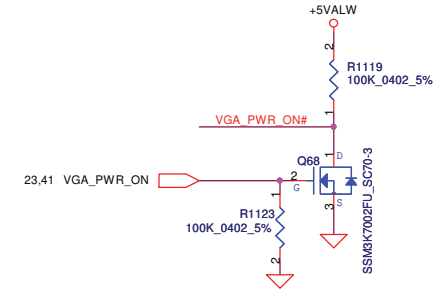
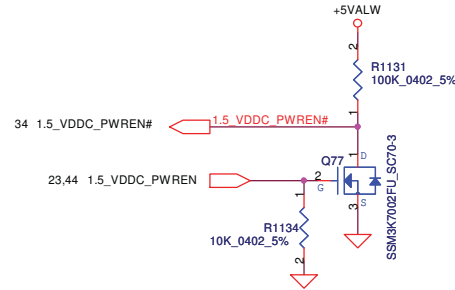
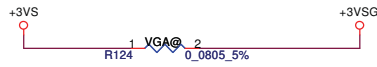
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

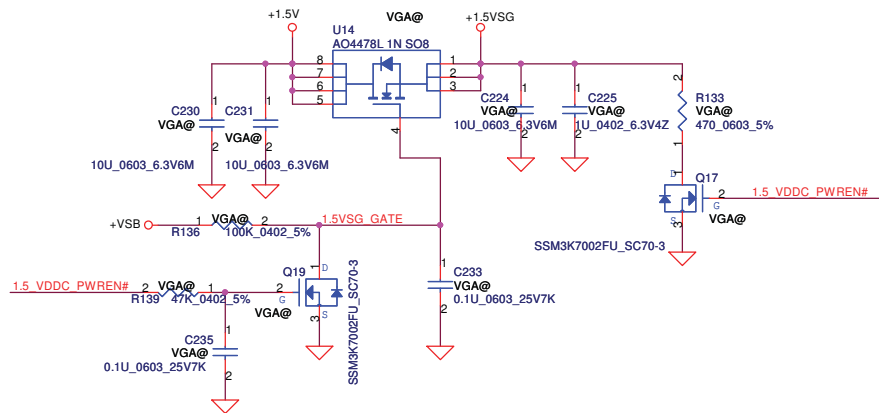
VGA_PWR_ON source signal	Seymour
+3.3VSG	VGA_ON
+1.8VSG	SUSP#
+1.0VSG	VGA_PWR_ON#
+VDDCI	VGA_PWR_ON
+VGA_CORE	Combine with +VGA_CORE
+1.5VSG	1.5_VDDC_PWREN
	1.5_VDDC_PWREN#



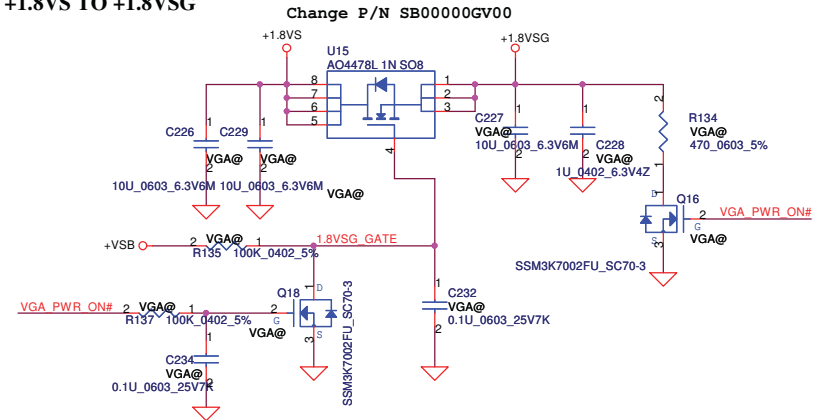
+3.3VS TO +3.3VSG



+1.5V TO +1.5VSG

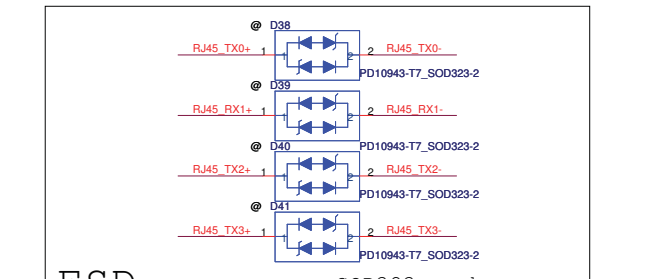
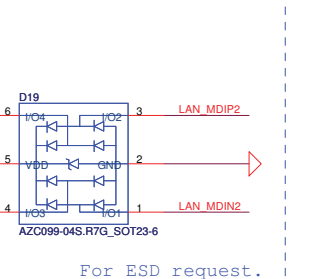
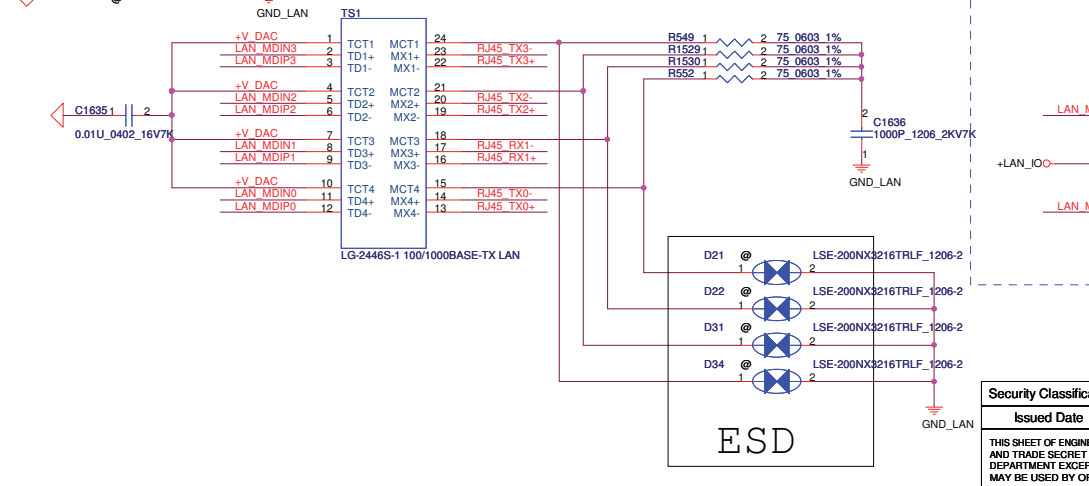
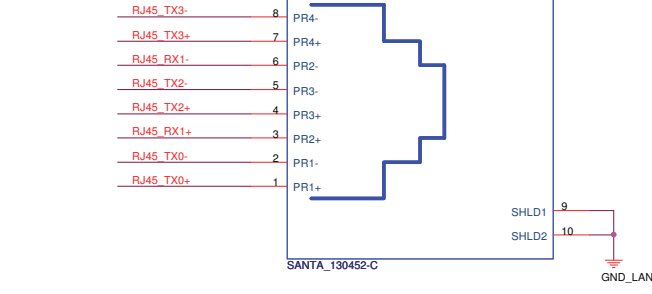
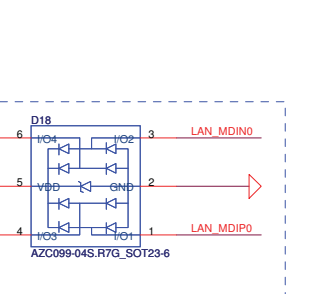
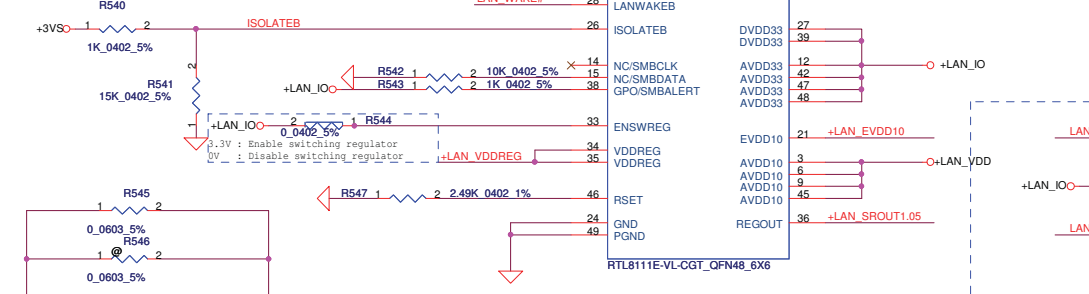
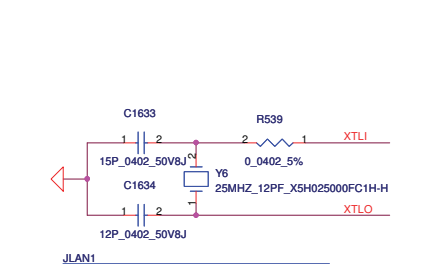
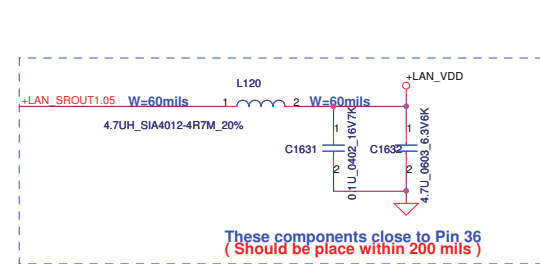
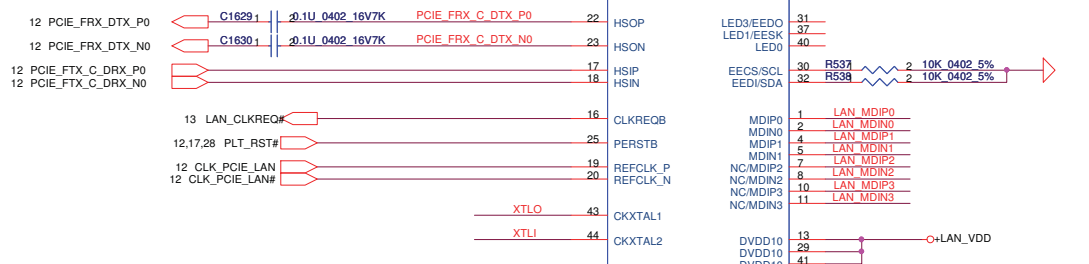
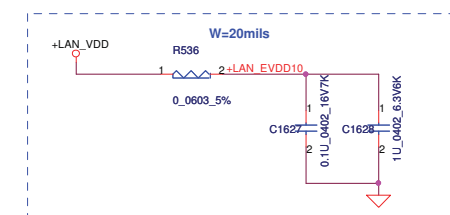
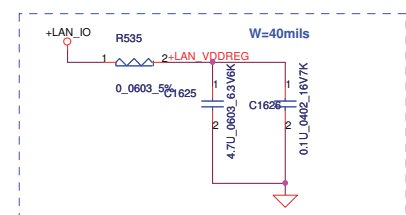
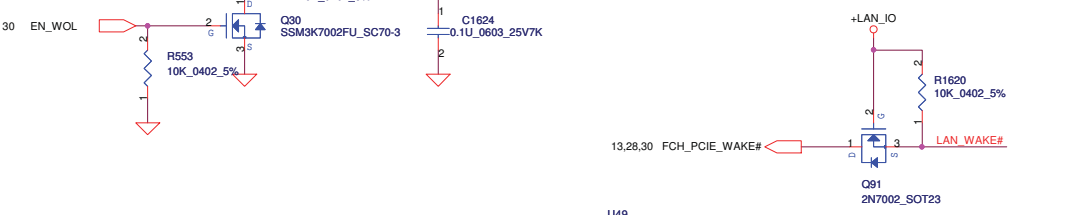
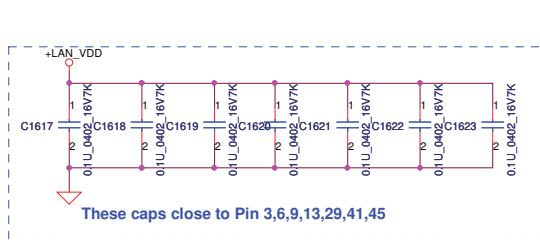
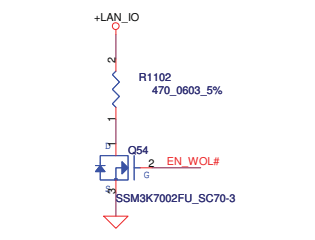
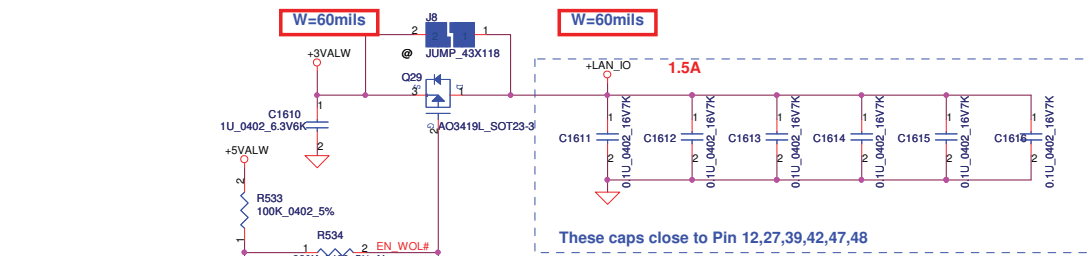


+1.8VS TO +1.8VSG

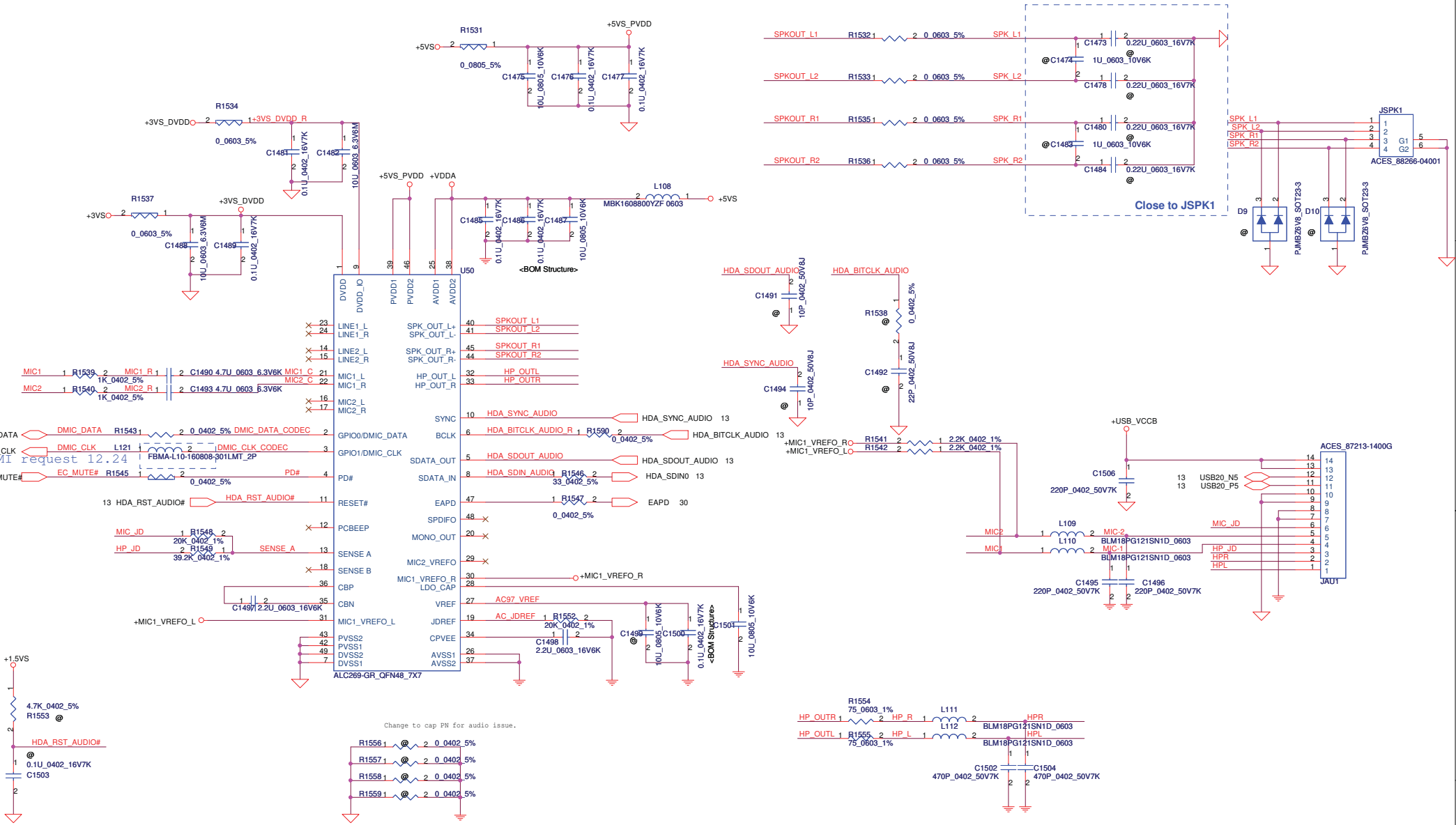


Change P/N SB00000GV00

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				P24-VGA DC Interface	
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		Customer	LA-7322P	Date:	Thursday, February 17, 2011
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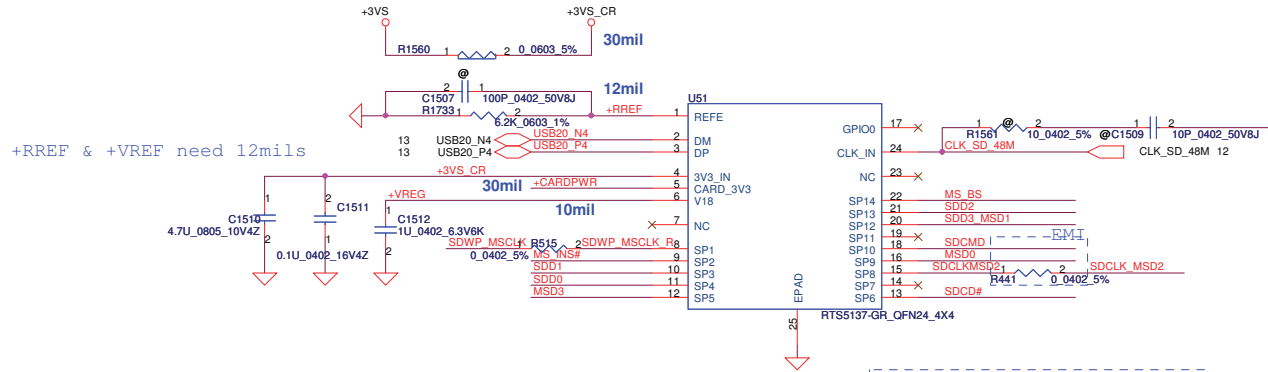


Change to cap PN for audio issue.

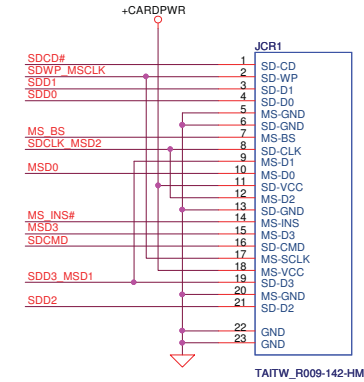
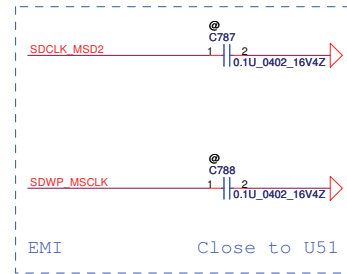
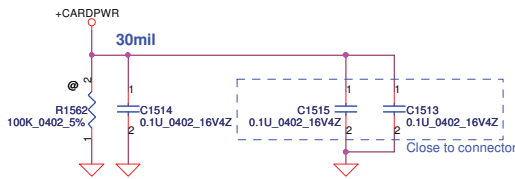
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Title		Compal Electronics, Inc.	
Size		P26-HD CODEC ALC259	
Customer	Document Number	Date	Rev
LA-7322P	LA-7322P	Thursday, February 17, 2011	1.0
Date		Sheet	26 of 47

Card Reader RTS5137 (only SD/MMC/MS function)



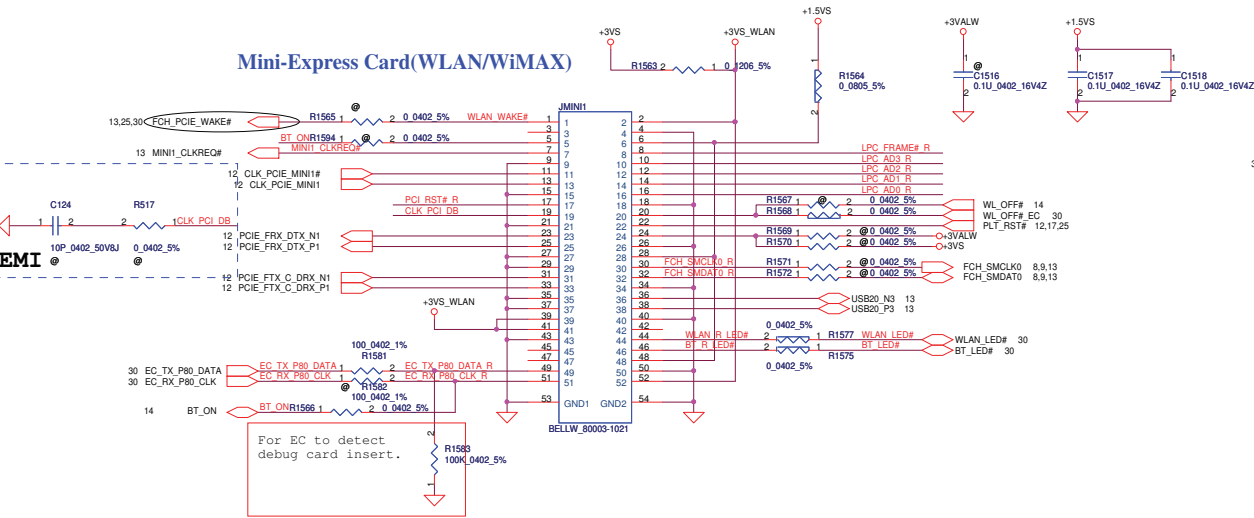
Card Reader Connector



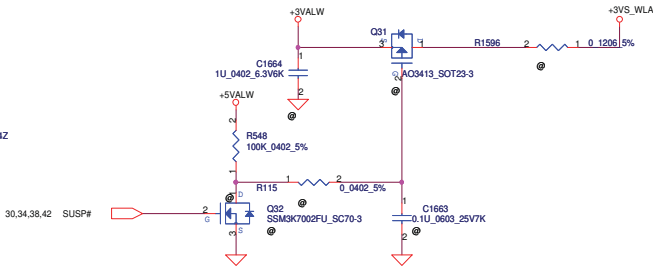
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Size	Document Number	Rev		Date	
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				Sheet	27 of 47

Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



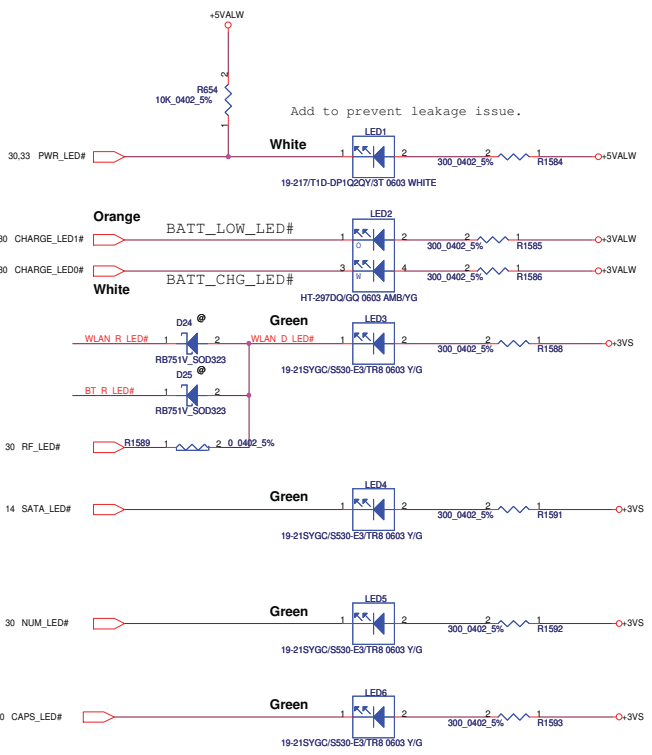
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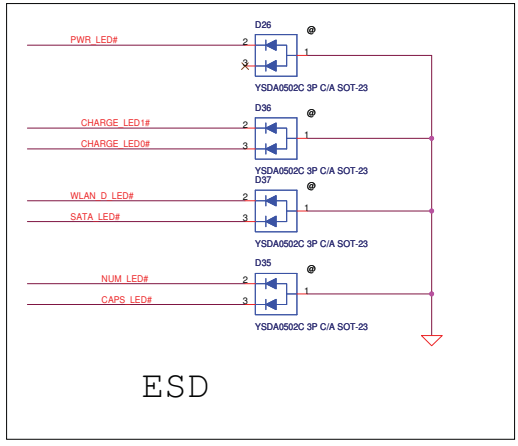
**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

LPC_FRAME# R	R1573	1	2	0.402 5%	LPC_FRAME#	12.30
LPC_AD3 R	R1574	1	2	0.402 5%	LPC_AD3	12.30
LPC_AD2 R	R1575	1	2	0.402 5%	LPC_AD2	12.30
LPC_AD1 R	R1576	1	2	0.402 5%	LPC_AD1	12.30
LPC_ADD0 R	R1577	1	2	0.402 5%	LPC_ADD0	12.30
LPC_ADD1 R	R1578	1	2	0.402 5%	LPC_ADD1	12.30
LPC_ADD2 R	R1579	1	2	0.402 5%	LPC_ADD2	12.30
LPC_ADD3 R	R1580	1	2	0.402 5%	LPC_ADD3	12.30
CLK_PCIE_DB					CLK_PCIE_DB	12

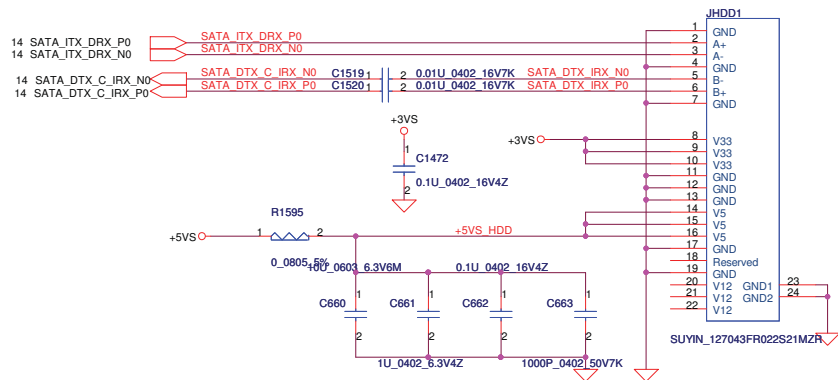
LED



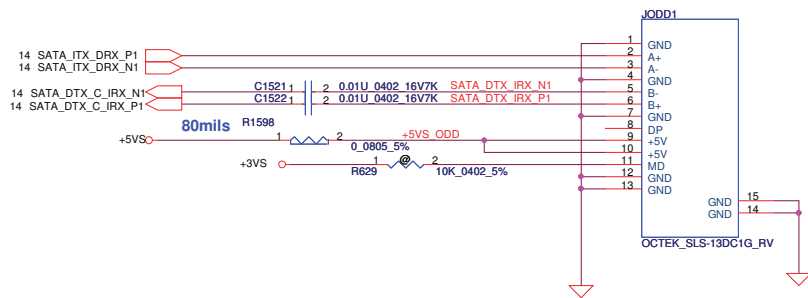
ESD



SATA HDD Conn.

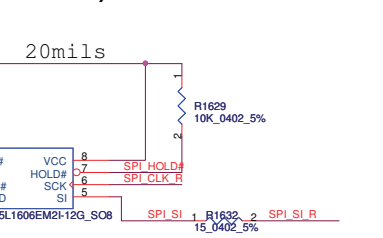
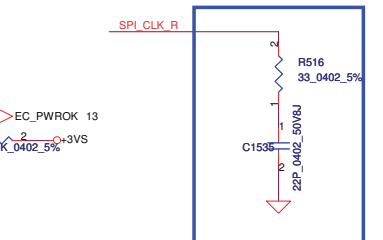
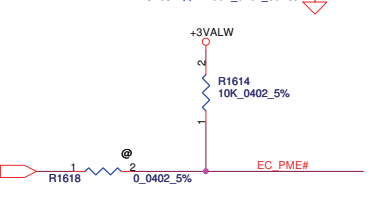
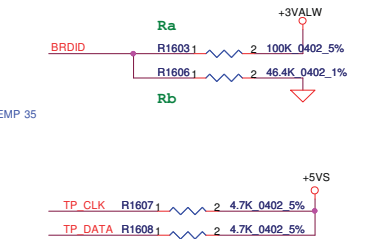
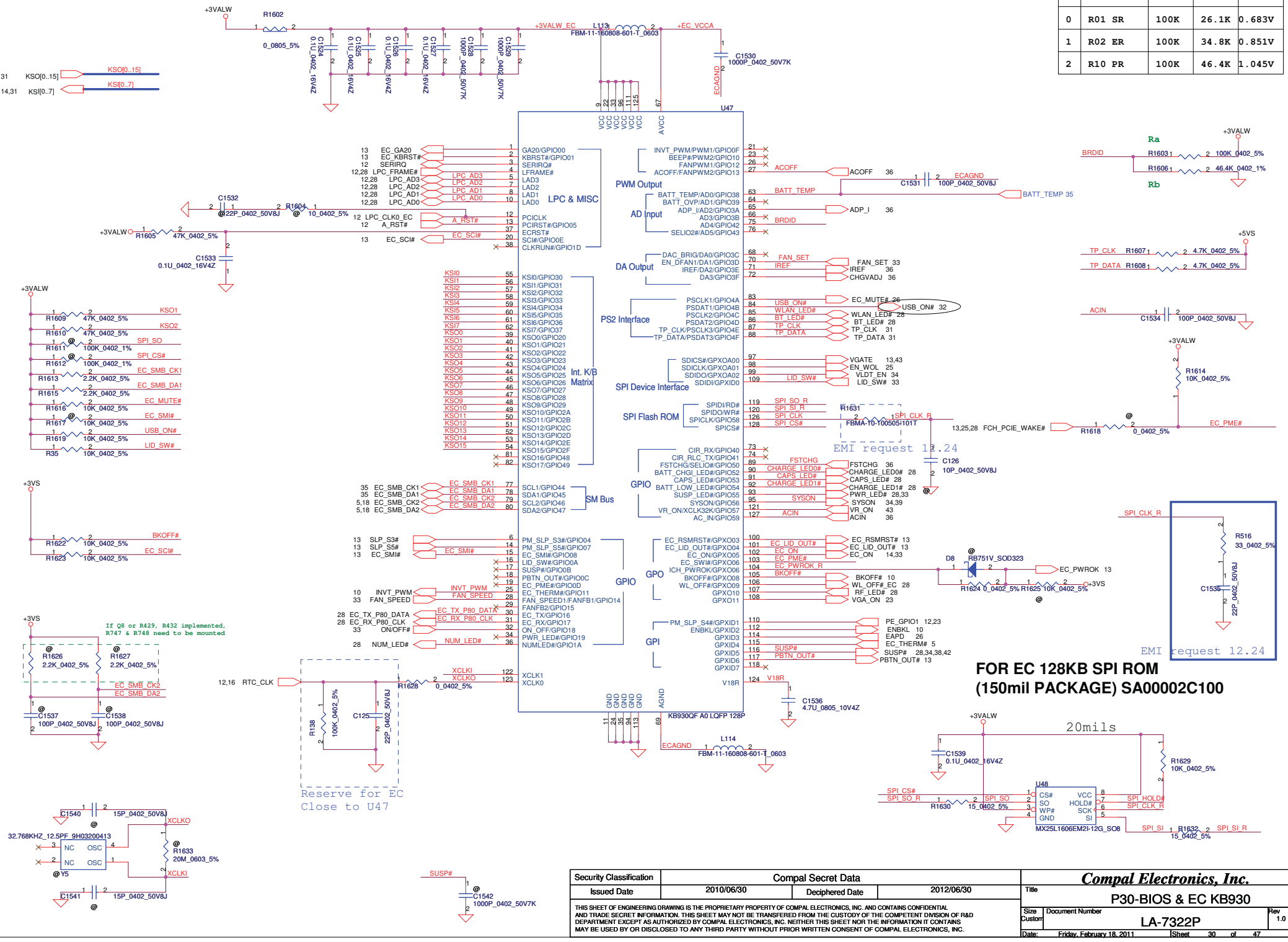


SATA ODD FFC Conn.



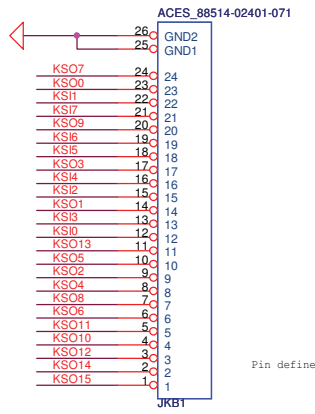
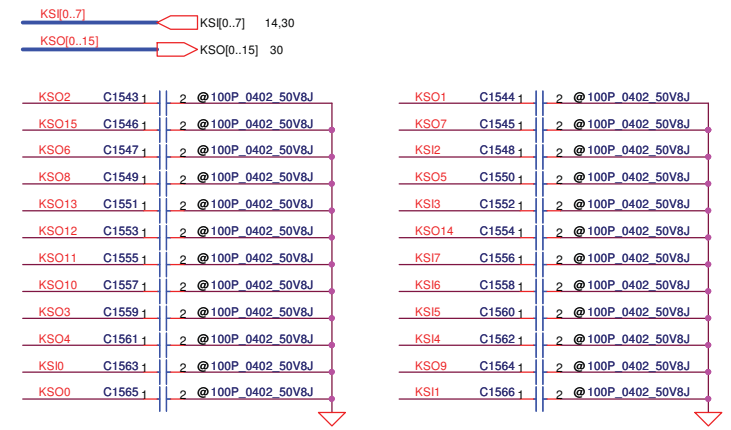
Security Classification		Compal Secret Data		Title		
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R10 PR	100K	46.4K	1.045V



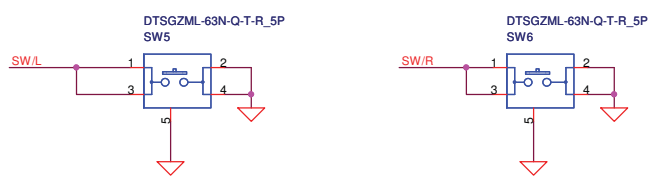
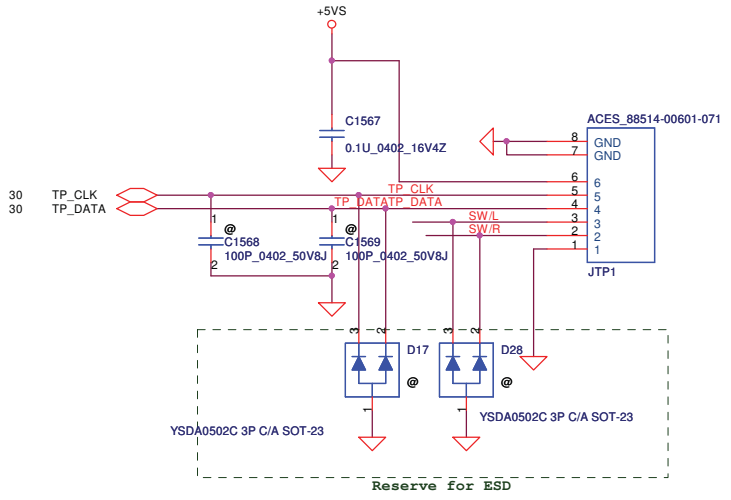
Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	P30-BIOS & EC KB930	
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INT_KBD Conn.

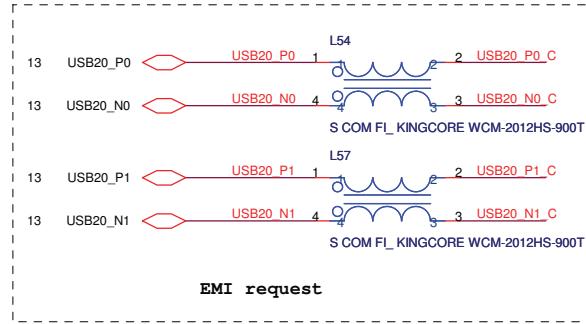


CONN PIN define need double check

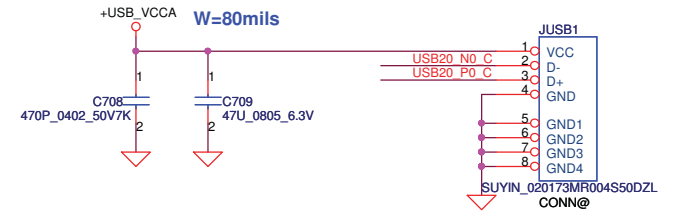
To TP/B Conn.



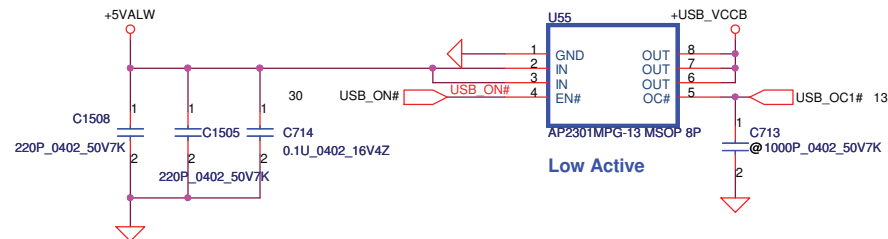
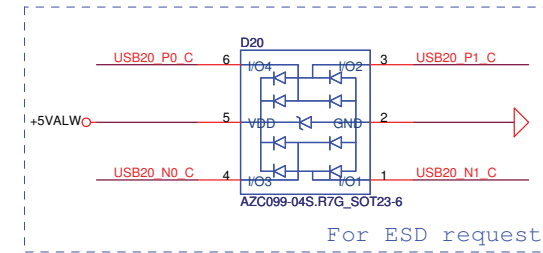
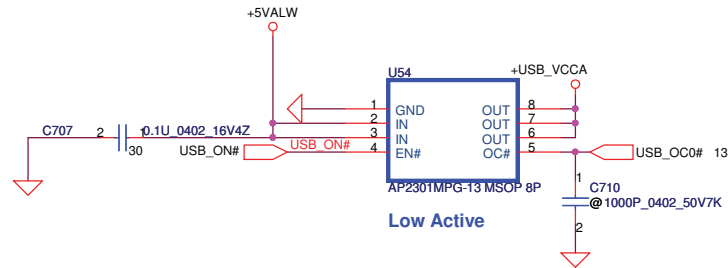
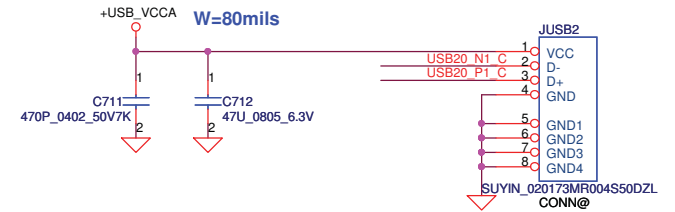
Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	P31-KB /SW/TP/Lid	
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Left USB Conn.

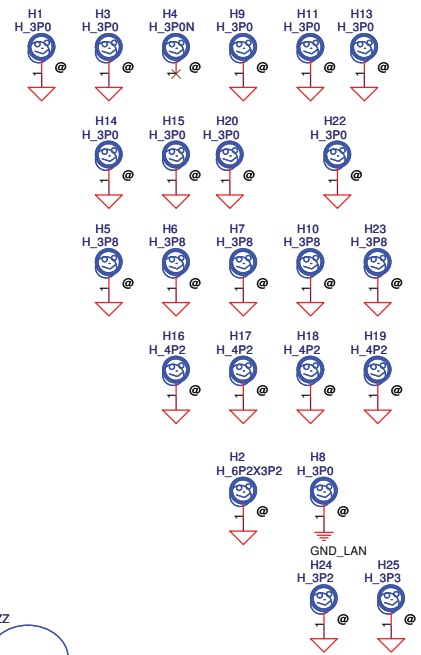
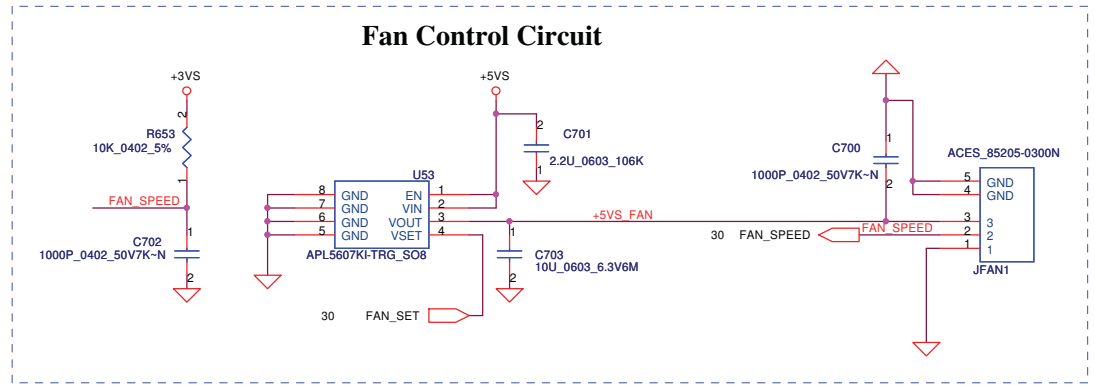
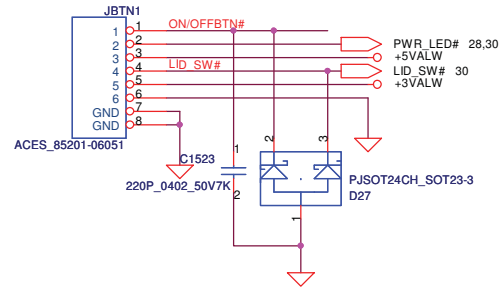
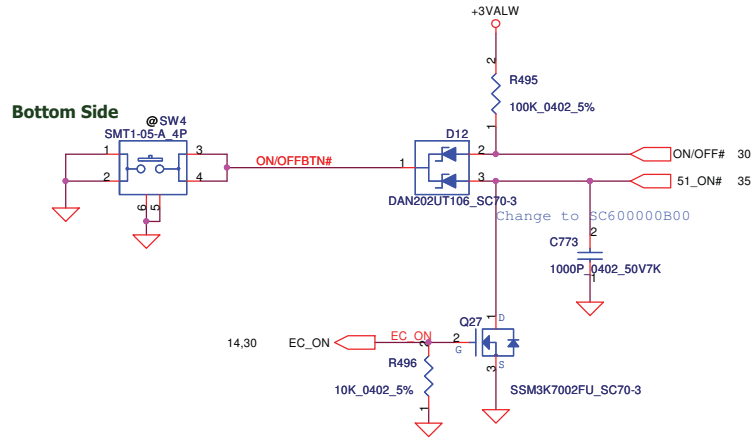


Left USB Conn.



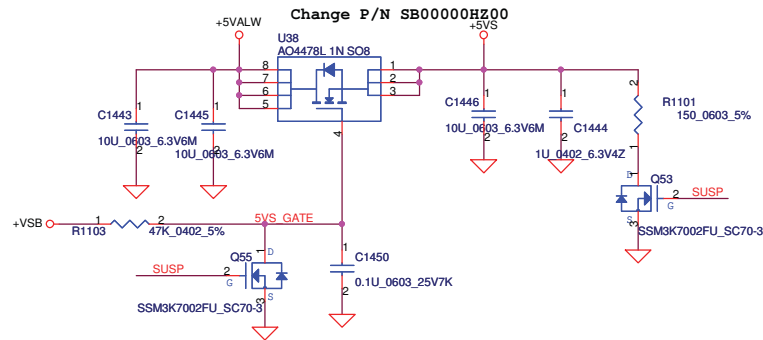
Security Classification		Compal Secret Data		Title Compal Electronics, Inc. P32-USB/BT/USBsub	
Issued Date	2010/06/30	Deciphered Date	2012/06/30		
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ON/OFF switch **Power Button**

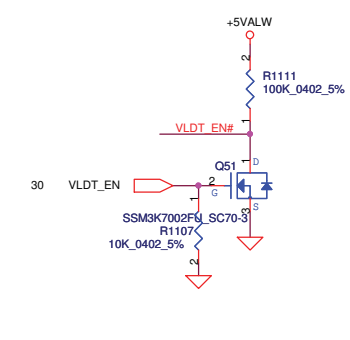
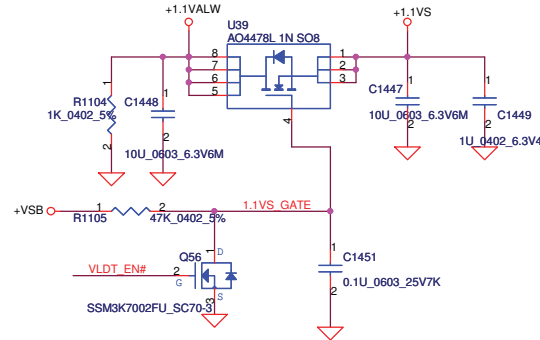


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+5VALW TO +5VS

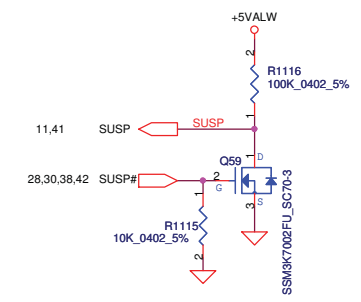
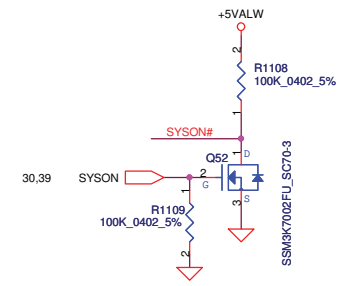
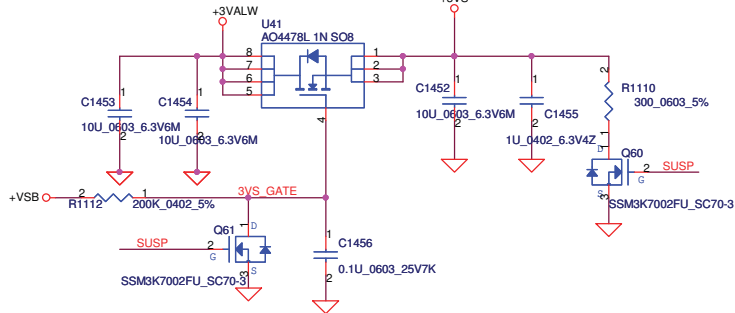


+1.1VALW TO +1.1VS

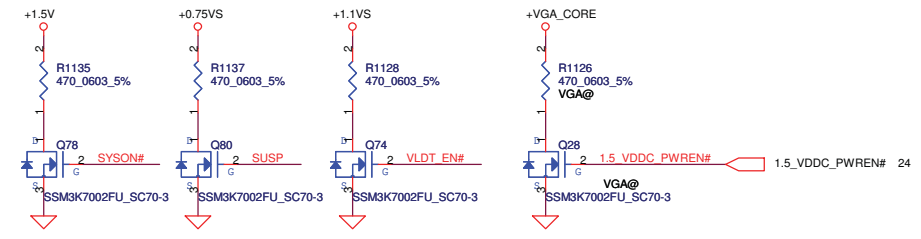
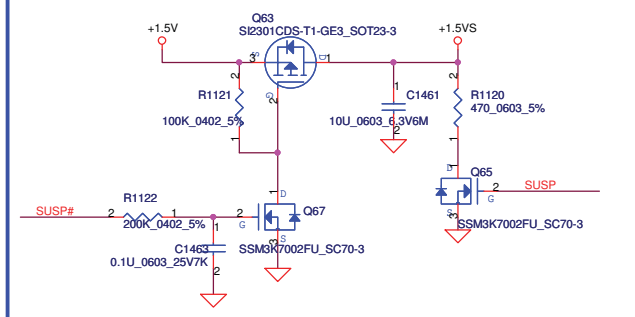


+3VALW TO +3VS

Change P/N SB00000HZ00

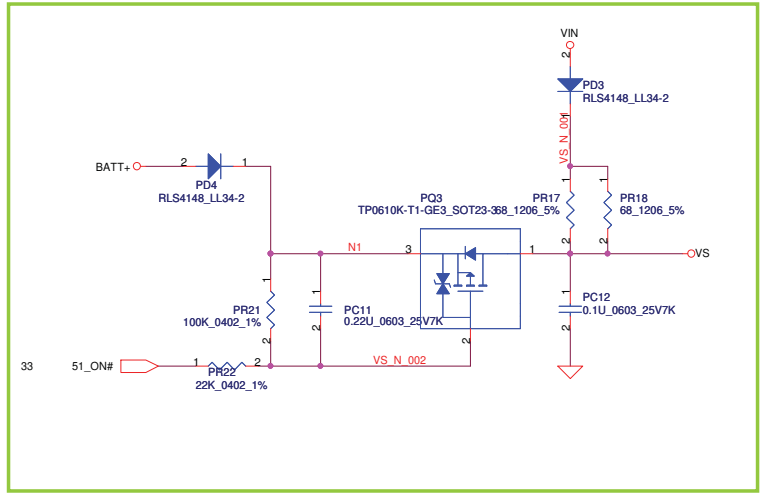
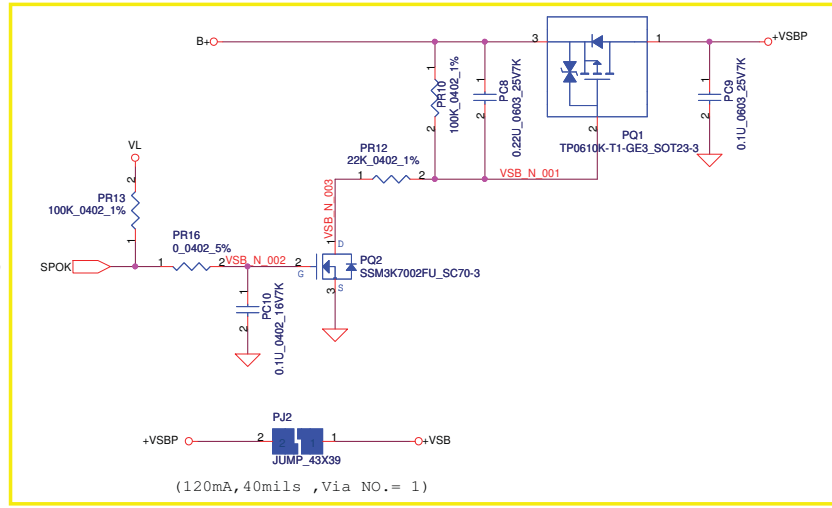
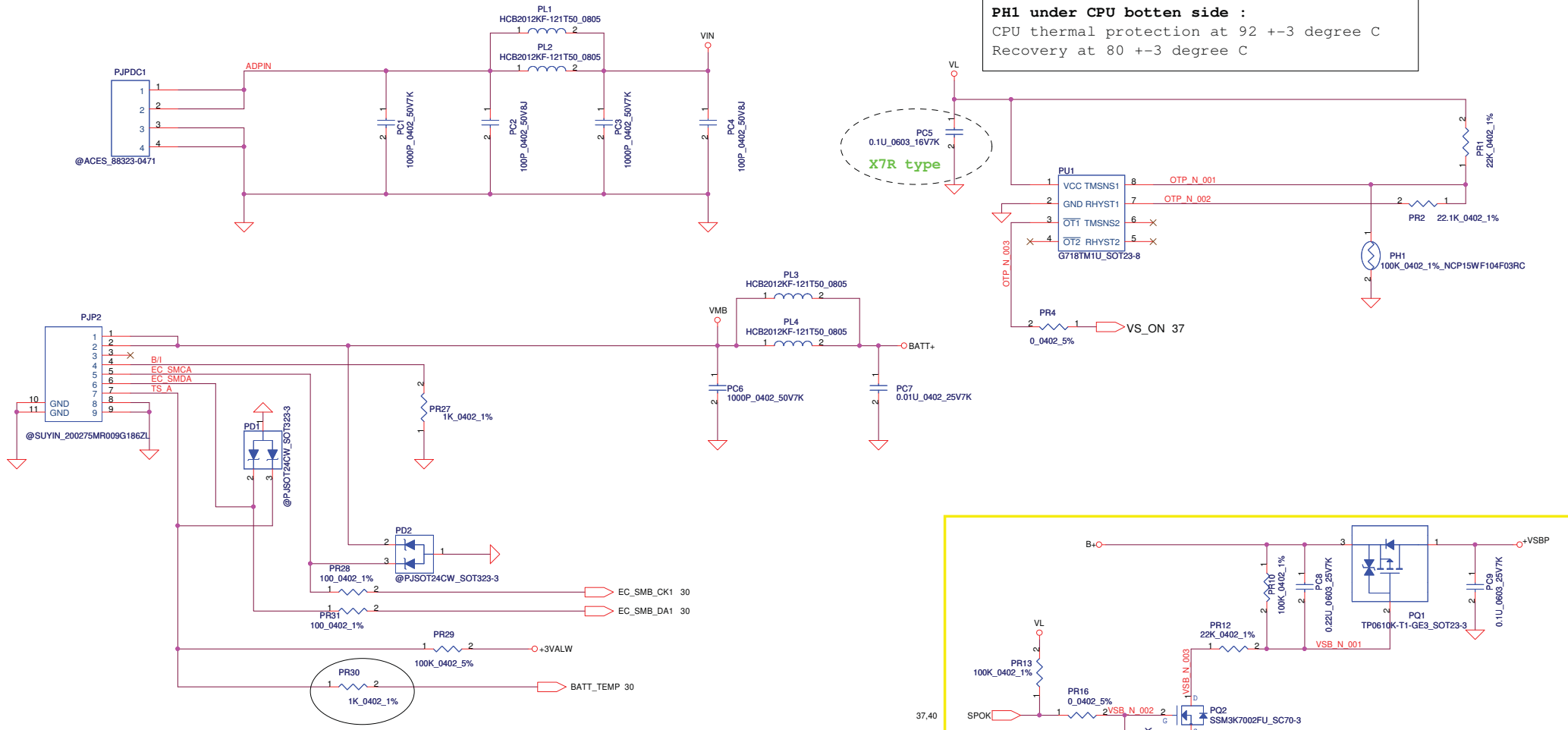


+1.5VS

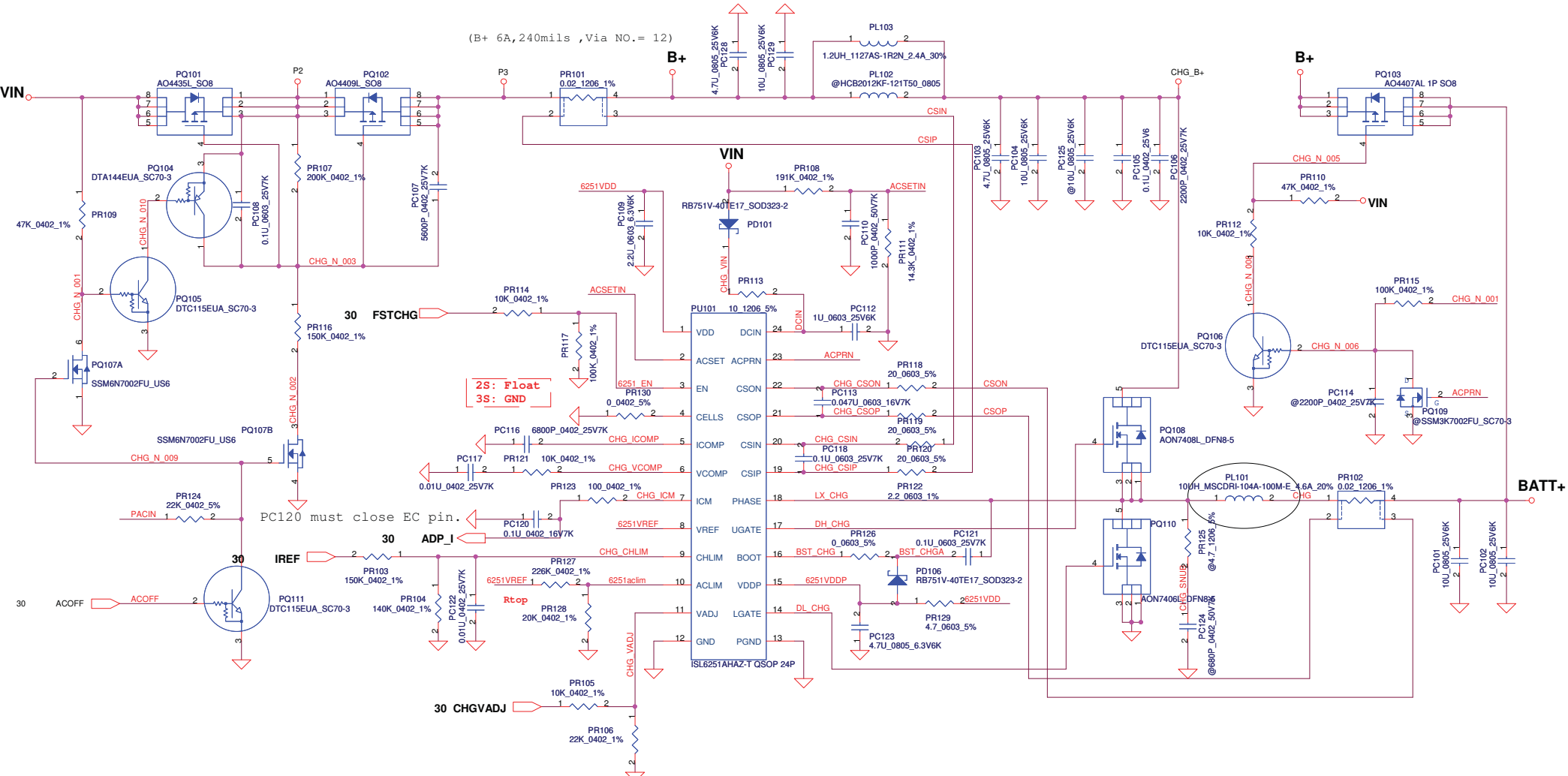


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				P34-DC Interface		
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PH1 under CPU botten side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C



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				DCIN / BATT CONN / OTP
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				0.1
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(B+ 6A, 240mils, Via NO.= 12)

2S: Float
3S: GND

PC120 must close EC pin.

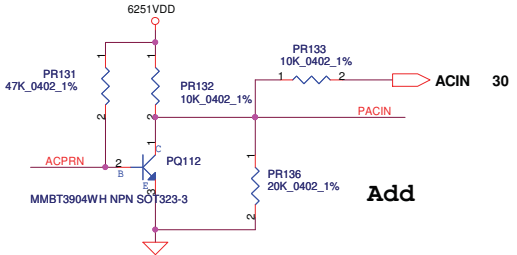
30 CHGVADJ

CP= 85%*Iada;
 Iada=0~4.737A (90W); CP=4.03A; where Racdet=0.020ohm, where Rtop=12.4K
 90W for Dis: Rtop: SD00000AJ80
 Iada=0~3.421A (65W); CP=2.91A; where Racdet=0.020ohm, where Rtop=226K
 65W for UMA: Rtop: SD034226380
 Astro2010_01_15 need confirm P/N

CP mode
 $Va_{clim} = VREF * (R_{bot} / (R_{internal} / (R_{top} / (R_{internal} + R_{bot}) / R_{internal})))$
 when 90W $Va_{clim} = 2.39 * (20K / (152K / (20K / (152K + 12.4K) / 152K))) = 1.44966V$
 when 65W $Va_{clim} = 2.39 * (20K / (152K / (20K / (152K + 226K) / 152K))) = 0.38914V$
 $I_{input} = (1 / Racdet) * ((0.05 * Va_{clim} / VREF) + 0.05)$
 when 90W, $I_{input} = (1 / 0.02) * (0.05 * 1.44966 / 2.39 + 0.05) = 4.02A$
 when 65W, $I_{input} = (1 / 0.02) * (0.05 * 0.38914 / 2.39 + 0.05) = 2.92A$

CC=0.25A~3A
 IREF=1.016*Icharge
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

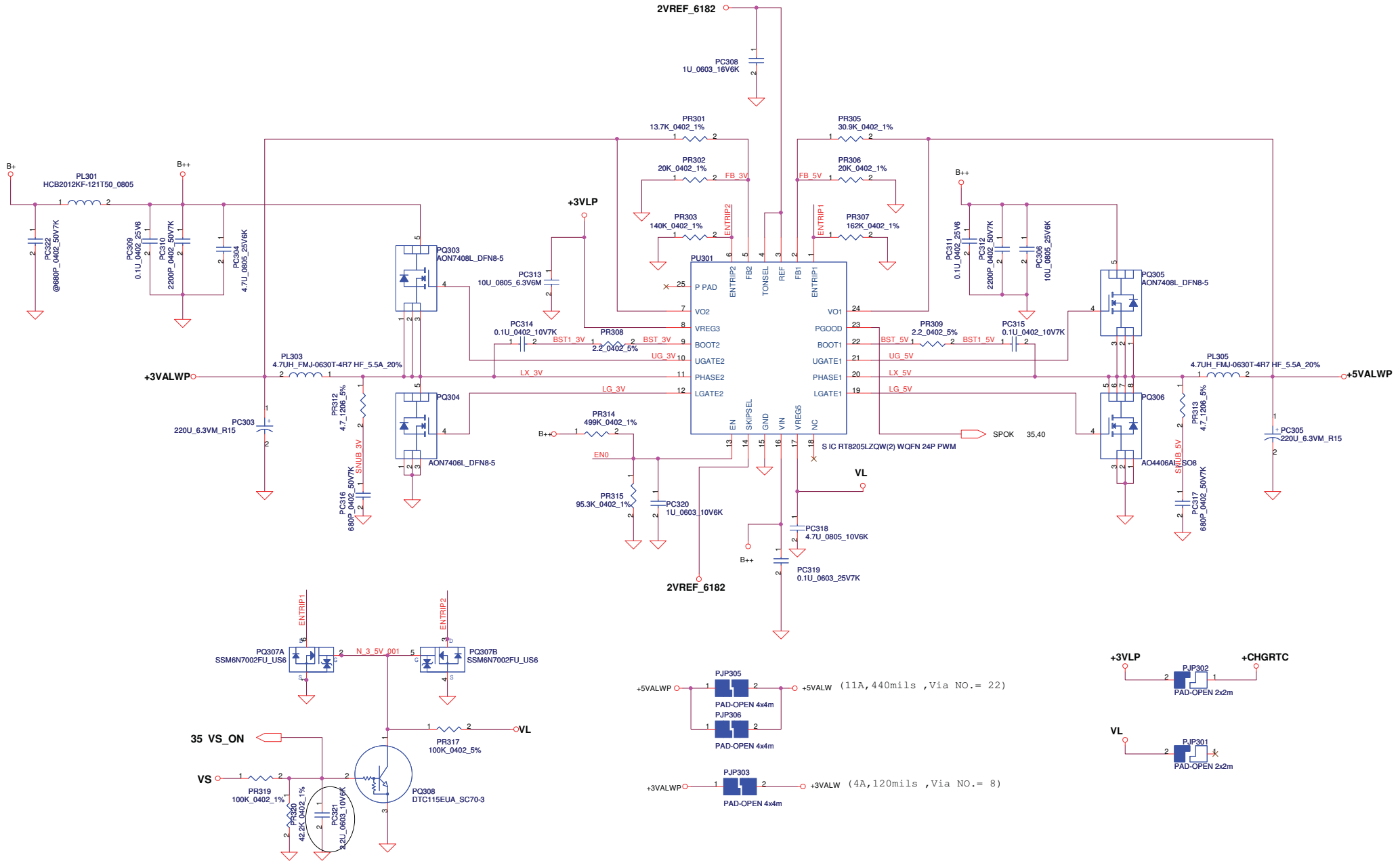
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V



Add

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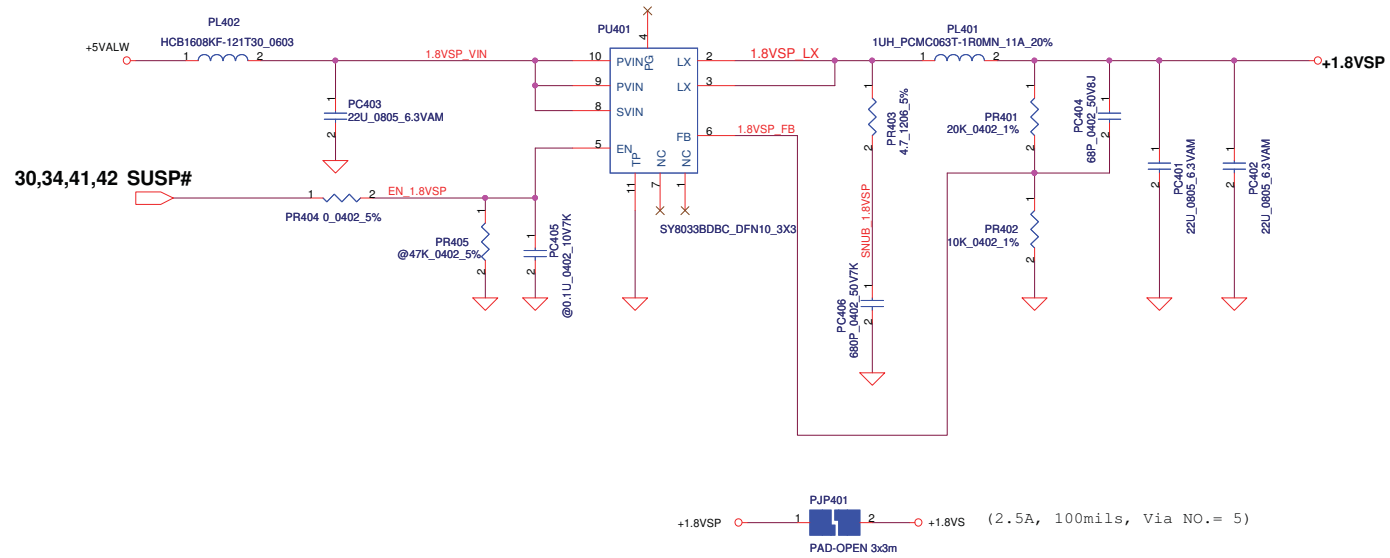
Compal Electronics, Inc.			
Title CHARGER			
Size	Document Number	Rev	
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EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data	
Issued Date	2007/08/02	Deciphered Date
		2008/08/02
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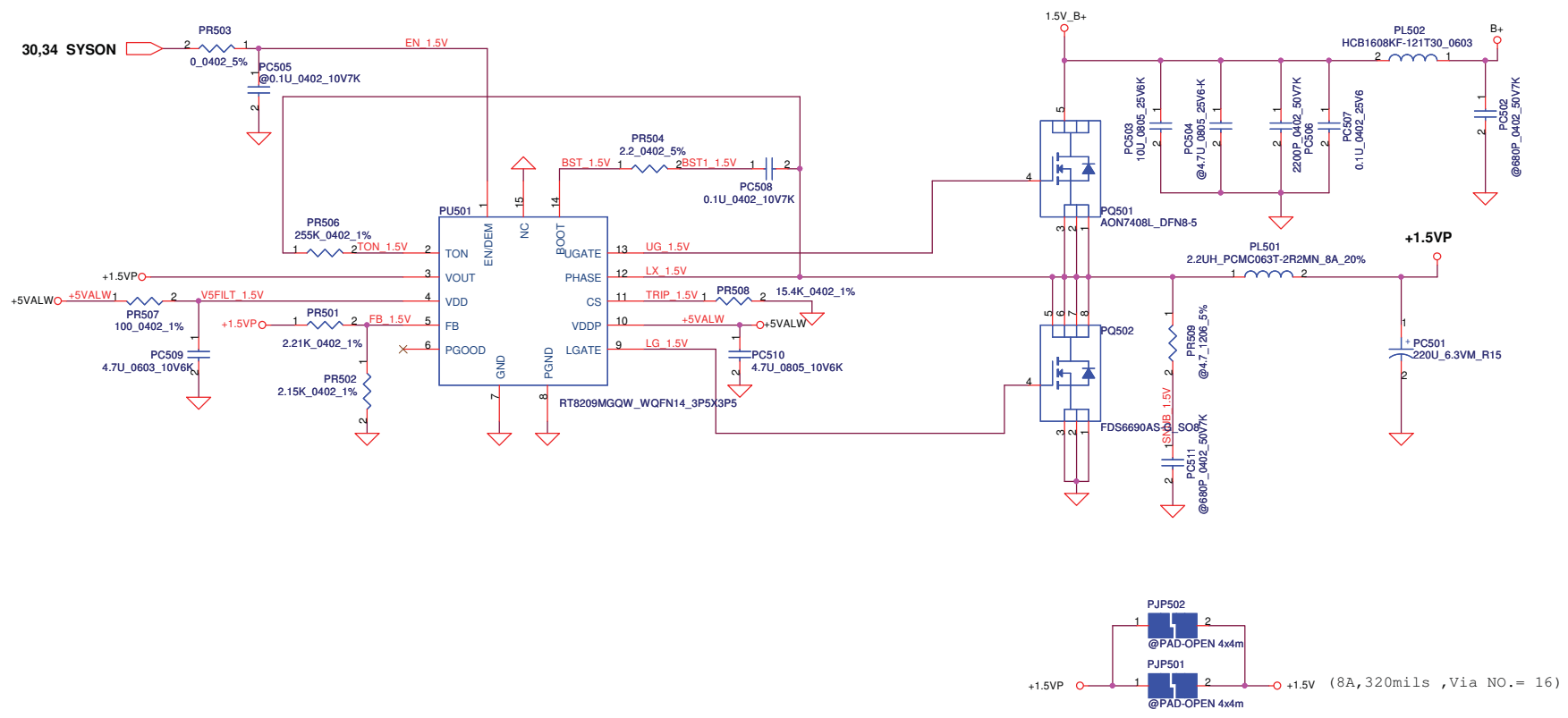
Compal Electronics, Inc.		
Title		
3.3VALWP/5VALWP		
Size	Document Number	Rev
Custort	LAXXXX	0.1
Date:	Friday, February 18, 2011	Sheet 37 of 44



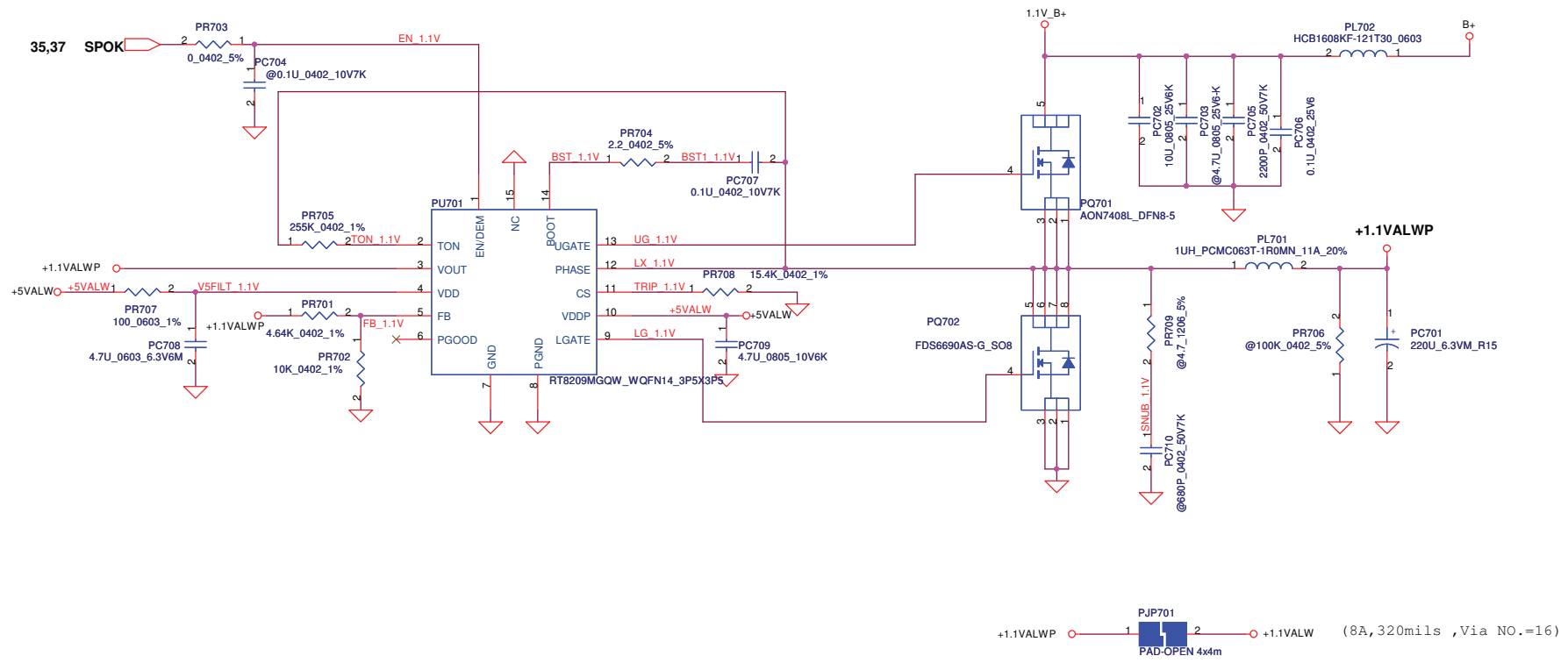
<Vo=1.8V> VFB=0.6V
 Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

30,34,41,42 SUSP#

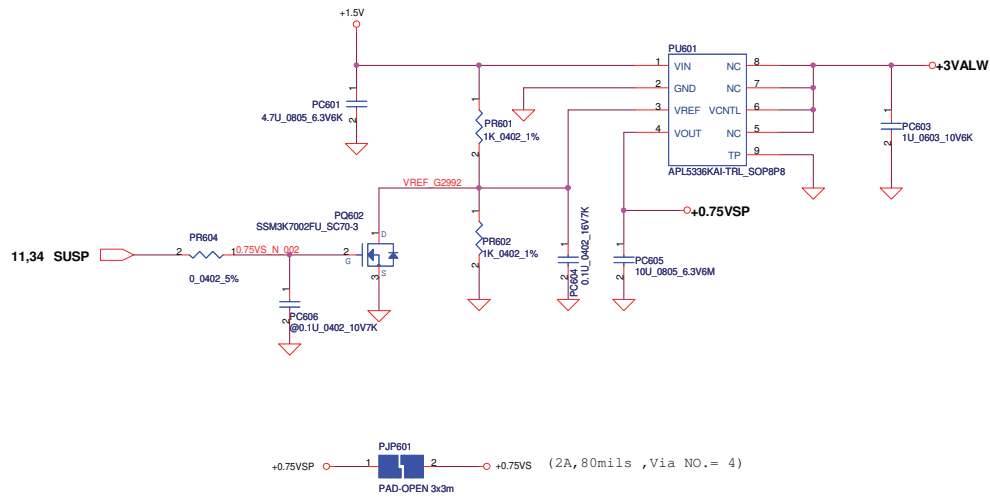
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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Size	Document Number			Rev	
	NCL61 LA-6321P M/B			0.1	
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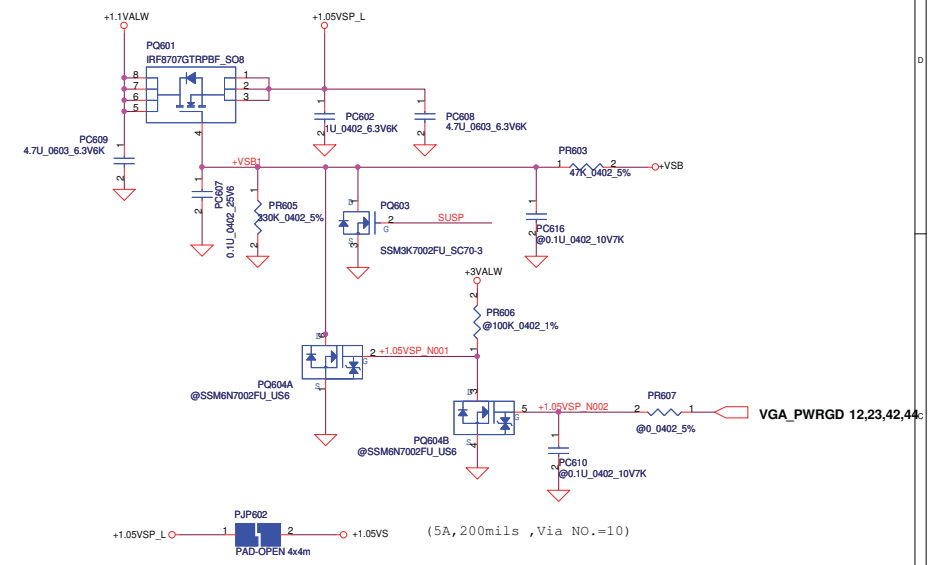
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	+1.5VP	
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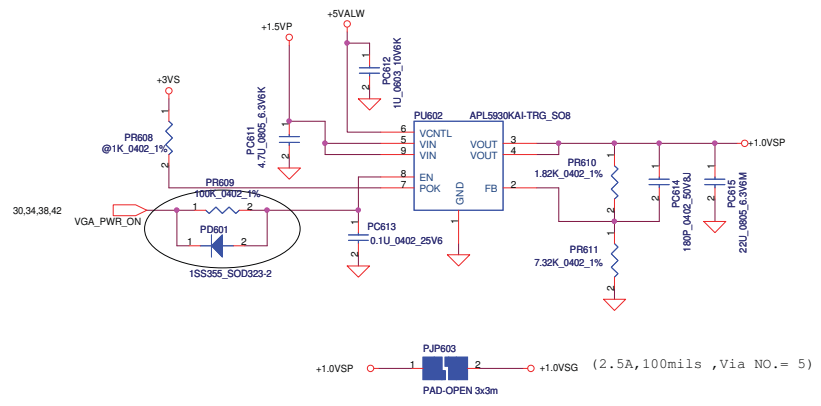
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR+1.1VALWP
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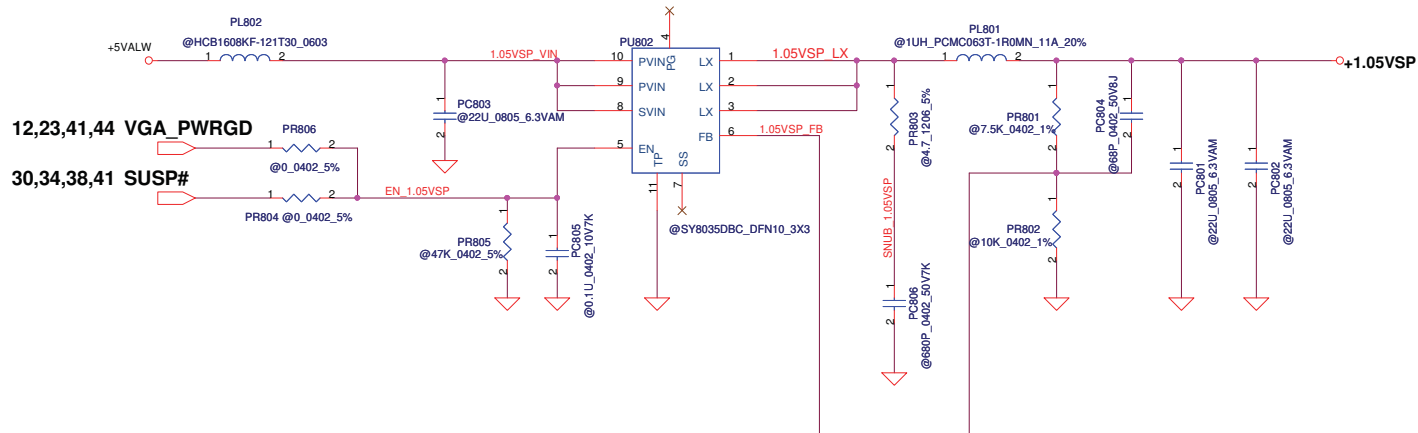
+1.1VALW TO +1.05VSP



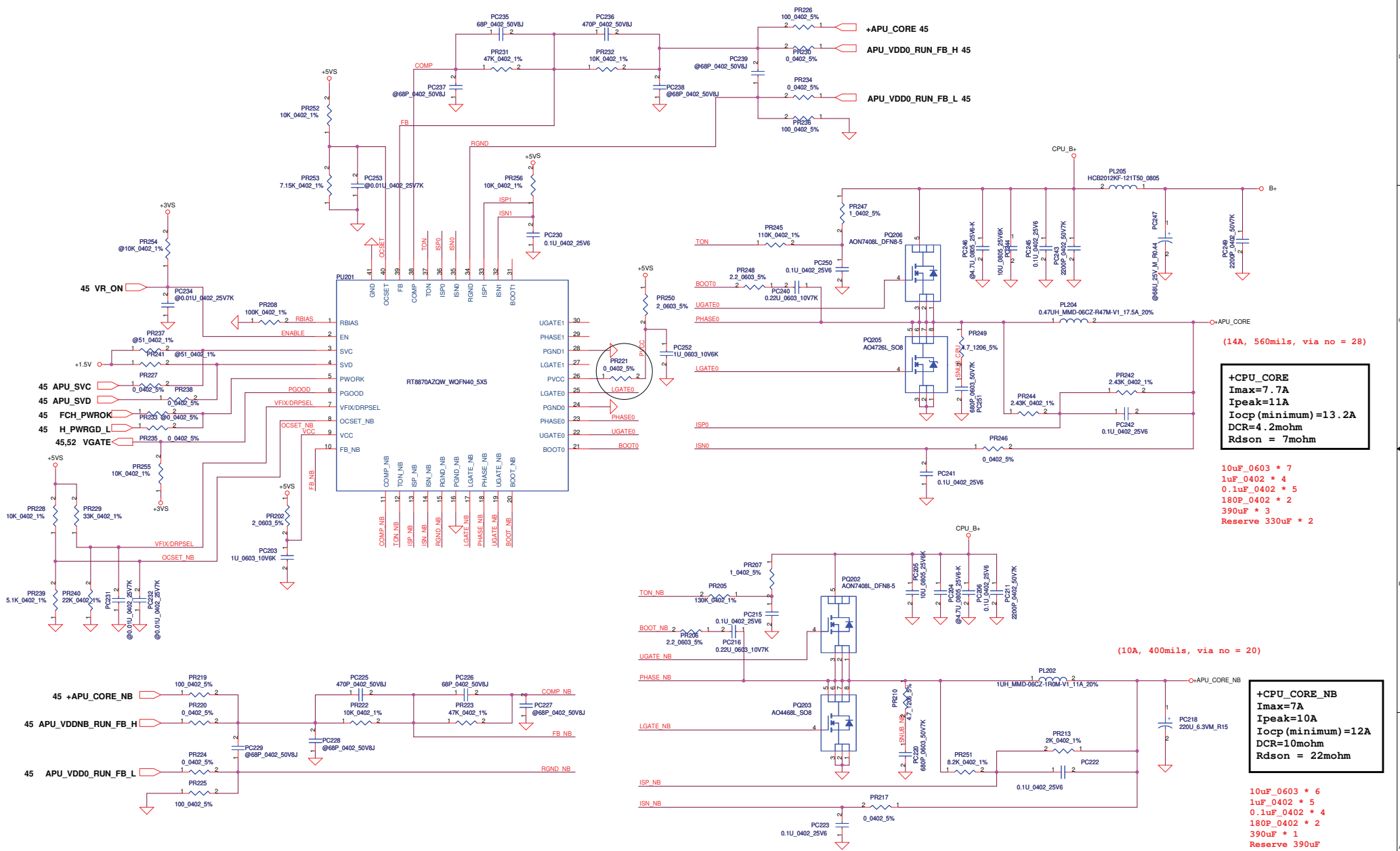
Need to confirm with HW power sequence.



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Size	Document Number			Rev	
	NCL61 LA-6321P M/B			0.1	
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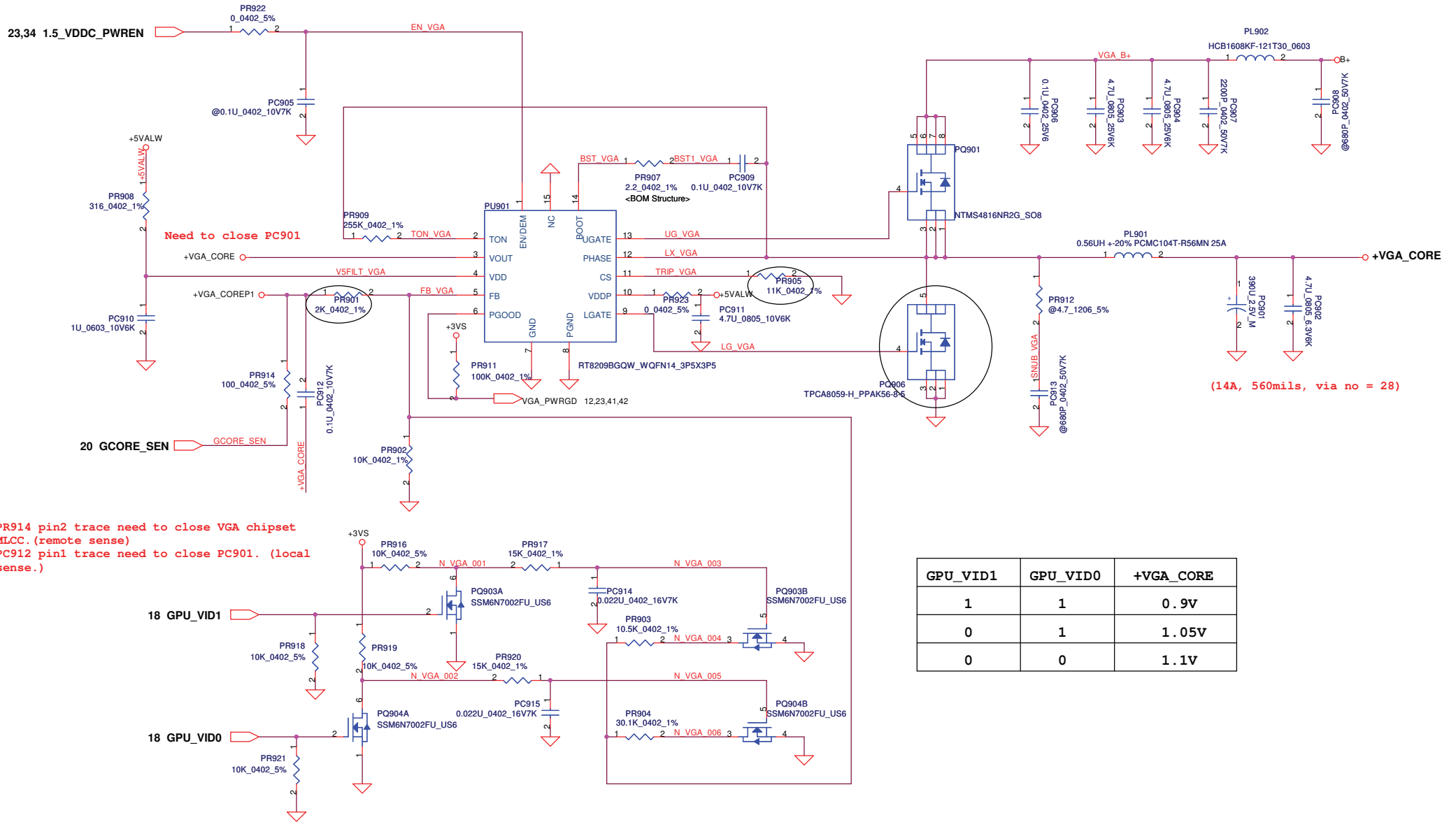


+CPU_CORE
I_{max}=7.7A
I_{ocp}(minimum)=13.2A
DCR=4.2mohm
R_{dson} = 7mohm

10uF_0603 * 7
 1uF_0402 * 4
 0.1uF_0402 * 5
 180P_0402 * 2
 390uF * 3
 Reserve 330uF * 2

+CPU_CORE_NB
I_{max}=7A
I_{ocp}(minimum)=12A
DCR=10mohm
R_{dson} = 22mohm

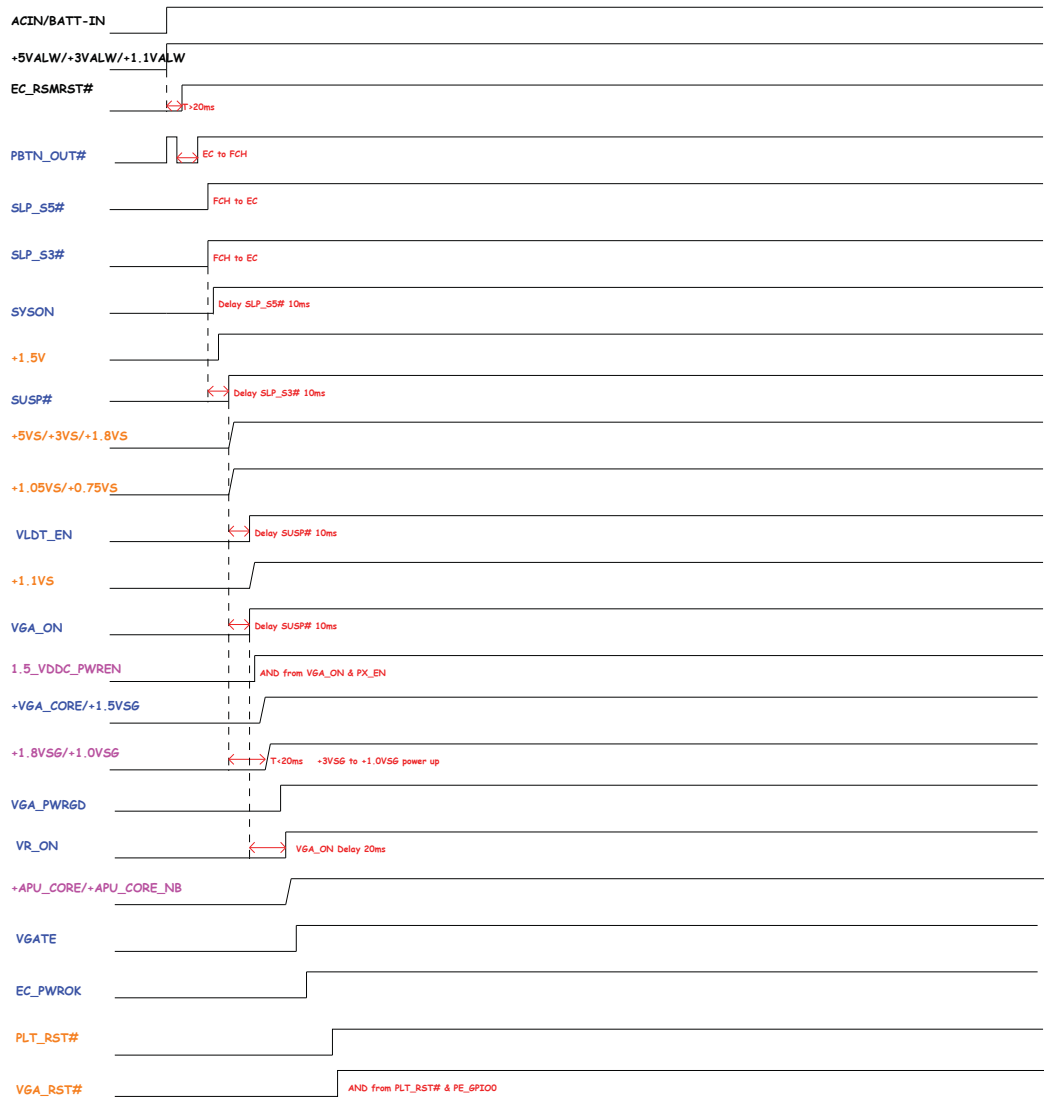
10uF_0603 * 6
 1uF_0402 * 5
 0.1uF_0402 * 4
 180P_0402 * 2
 390uF * 1
 Reserve 390uF



PR914 pin2 trace need to close VGA chipset MLCC. (remote sense)
 PC912 pin1 trace need to close PC901. (local sense.)

GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

POWER SEQUENCE



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		TP FFC error	0.11	PG#31	Swap JTP1 pin define	12/15	ER
2		SW5 SW6 footprint error	0.11	PG#31	Update SW5 SW6 footprint	12/15	ER
3		FAN module connecter pin define error	0.11	PG#33	Swap JFAN1 pin define	12/15	ER
4		DFB request to update footprint	0.11	PG#26 PG#33	Update JBTN1& JSPK1 footprint	12/15	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/15	ER
6		LID issue	0.11	PG#30	LID_SW# added a pull up 10Kohm. (R35)	12/15	ER
7		Update Broad ID	0.11	PG#30	Change R1606 from 26.1Kohm to 34.8Kohm	12/15	ER
8		Double component	0.11	PG#34	Del Q54 & R1102	12/15	ER
9		Update PW schematic	0.11			12/16	ER
10		APU_THERMTRIP# of FCH SPEC	0.11	PG#05	R424 & Q79 change to unpop, R427 change to pop	12/17	ER
11		EC release note	0.11	PG#30	Add C125 & R138	12/17	ER
12		Crisis circuit	0.12	PG#14	Add UH6,R512,R513,R514	12/20	ER
13		DDR3 SPD	0.12	PG#08	Reserve R155 R152	12/21	ER
14		Update PW schematic	0.13			12/23	ER
15		Clear CMOS	0.13	PG#12	R865 change to CLRP1	12/23	ER
16		Procurement recommend	0.13		D4,Q97,Q29 change PN & footprint	12/23	ER
17		WLAN PW spec	0.13	PG#28	Reserve Q31 ,Q32 circuit	12/24	ER
18		EMI request	0.13	PG#26	R1544 change to L121	12/24	ER
19		EMI request	0.13	PG#30	R1631 change to FBMA-10-100505-101T	12/24	ER
20		EMI request	0.13	PG#30	R516 change to 33ohm, C1535 change to 22P	12/24	ER
21		LAN power	0.13	PG#25	Add R553 & J8	12/27	ER
22		EMI request	0.13	PG#25	R549,R552,R1529,R1530 change to 0603	12/27	ER
23		Update PW schematic	0.13			12/27	ER
24		Crystal EA	0.2	PG#18	C35,C36 change to 18P from 20P	12/29	ER
25		Crystal EA	0.2	PG#25	C1634 change to 10P from 27P C1633 change to 12P from 27P	12/29	ER
26		Crystal EA	0.2	PG#12	C66 change to 8.2P from 22P C67 change to 10P from 22P	12/29	ER
27		PE_GPIO1 pull down	0.2	PG#12	Add R109 for PE_GPIO1	12/29	ER

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				Custom	1.0
				LA-7322P	
				Date:	Thursday, February 17, 2011
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
28		Discharge time fail.	0.21	PG#34	Change R1110, R1101 from 470 ohm to 300 ,150 ohm.	01/11	ER
29		For frequency matching.	0.21	PG#12	Change Y4 from 12.5pF to 7 pF Change C64,C65 from 22p to 10pF.	01/11	ER
30		For CRT EA.	0.21	PG#10	Change C1572,C1573,C1574,C1575,C1576,C1577 from 10p to 6.8p. Change bead value.	01/11	ER
31		Change the strap for RAM.	0.21	PG#08 PG#09	Pop R153 and R155, un-pop R961,R150.	01/11	ER
32		Correct HDMI audio strap pin.	0.21	PG#18	Un-pop R21,R22 for DIS skew.	01/11	ER
33		Reserve for S3 can't be resume issue of some APU.	0.21	PG#06	Add R1705,R1706.	01/21	PR
34		For PR phase ME assemble.	0.21	PG#33	Del SW3 ,Unpop Sw4.	02/09	PR
35		For PR phase board ID.	0.22	PG#30	Change BID R1603 from 34.8k to 46.4k.	02/14	PR
36		For S3 resume fail issue.	1.0	PG#18	Add R75 1M ohm.	02/15	PR
37		For frequency matching.	1.0	PG#12	Change C66,C67 from 8.2pF 10pF p to 10pF 12pF.	02/16	PR
38		For frequency matching.	1.0	PG#25	C1634 change from 10P to 12P C1633 change from 12P to 15P	02/16	PR
39		For EMI test.	1.0	PG#32	Add C1508, C1505 220p.	02/17	PR
40		For EMI test.	1.0	PG#33	Add C1523 220p.	02/17	PR
41		For EMI test.	1.0	PG#26	Add C1506 220p.	02/17	PR
42		For only footprint.	1.0	PG#11	Del L11, L12, L13, L14	02/17	PR
43		For CRT EA.	1.0	PG#10	Change L116,L117,L118	02/17	PR
44			1.0	PG#10	Change R606 from 2.2k to 150 ohm.	02/17	PR
45		For LAN EMI test.	1.0	PG#25	Change TS1 from XXXXXX to SP050005L00	02/17	PR
46		For EMI request.	1.0	PG#30	Add C126 10 pF,change R516 to 39 ohm, C1535 to 33 pF.	02/17	PR
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