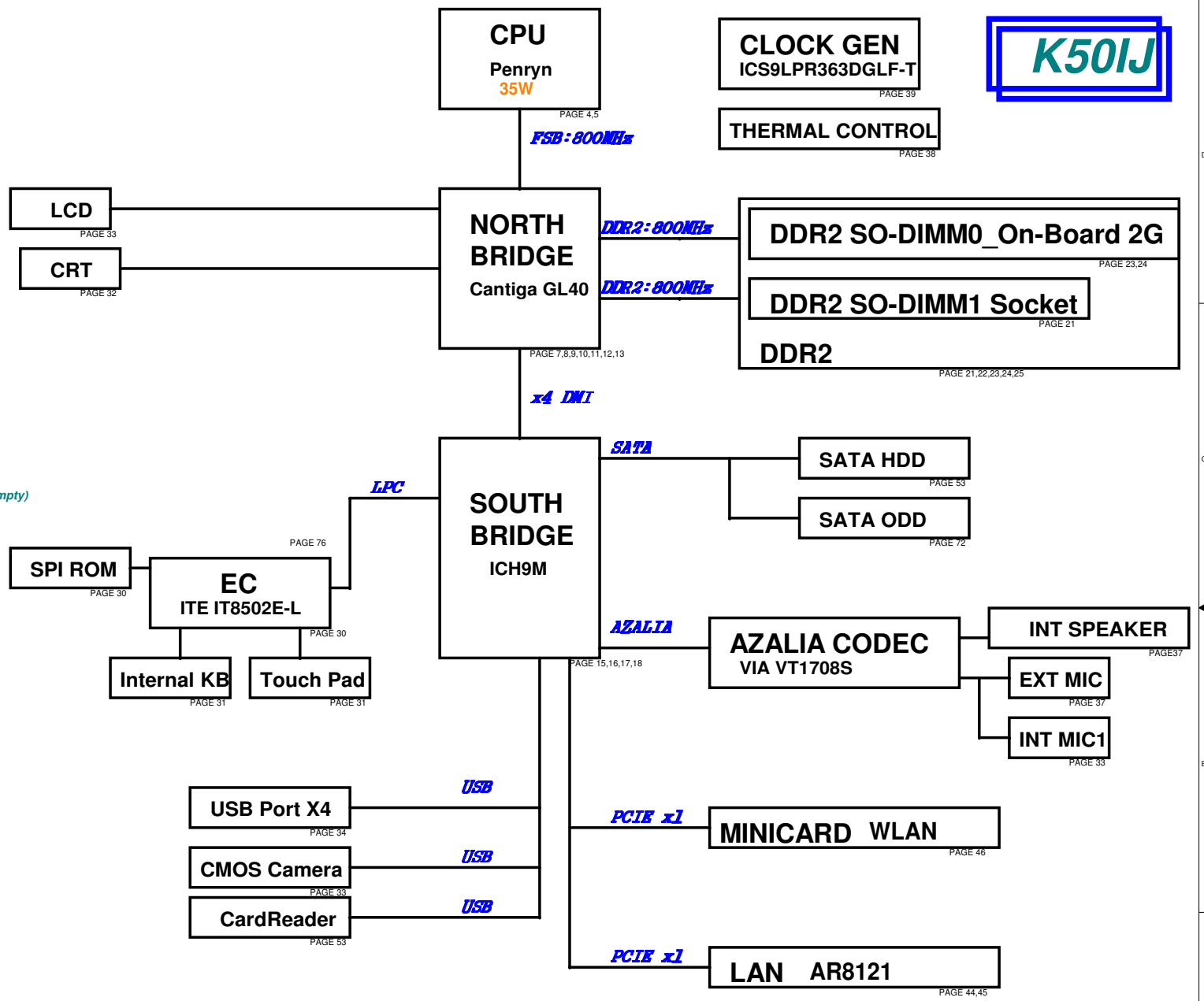


01	Block Diagram	61	*
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03	POWER SEQUENCE	63	*
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05	CPU-Penryn(PWR)	65	*
06	*	66	*
07	Cantiga(HOST)	67	DEBUG CONN
08	Cantiga(DMI & CFG)	68	DC & BAT IN
09	Cantiga(GRAPHIC)	69	*
10	Cantiga(DDR2)	70	*
11	Cantiga(PWR)	71	*
12	Cantiga(PWR2)	72	SATA-HDD & ODD
13	Cantiga(GND)	73	*
14	*	74	HOLE & Spring
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19	*	79	*
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22	DDR2 TERMINATION	82	POWER_I/O_1.5VS & 1.05VS
23	*	83	POWER_I/O_DDR & VTT
24	*	84	POWER_I/O(Empty)
25	*	85	POWER_VGA_CORE&1.1VS(Empty)
26	*	86	POWER_MCH_CORE(Empty)
27	*	87	POWER_CHARGER
28	*	88	POWER_DETECT
29	*	89	POWER_LOAD SWITCH
30	EC_IT8512E-L(1/2)	90	POWER_PROTECT
31	EC_IT8512E-L(2/2)	91	POWER_SIGNAL
32	CRT	92	POWER_FLOWCHART
33	LVDS & INVERTER CONNECTOR	93	POWER_HISTORY
34	BT		
35	*		
36	CONEXANT CX20582		
37	CONEXANT_HP/MIC		
38	THER SENSOR & FAN		
39	CLOCK GEN-ICS9LPR363DGLF-T		
40	*		
41	Switch Button & LED		
42	DISCHARGE		
43	*		
44	PCI-E LAN_RTL8111C		
45	MDC & RJ45+11		
46	Mini card_WLAN+3G		
47	*		
48	*		
49	*		
50	*		
51	*		
52	*		
53	CardReader & SIM CONN & TPM		
54	NEWCARD		
55	*		
56	HDA level shifter		
57	iHDMI		
58	*		
59	*		
60	*		



ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#EXT PU	+5VS
GPIO 06	GPI	- EXT PU	+3VS
GPIO 07	GPO	SEL_VID2 -	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	SUS_PWR_ACK EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI)	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLEPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO)	+3VS
GPIO 18	GPO	SEL_VID3 -	+3VS
GPIO 19	GPO	SEL_VID0 -	+3VS
GPIO 20	GPO	SEL_VID4 - INT PD*	+3VS
GPIO 21	GPO	VID_SW - High Active	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	SEL_VID5	+3VSUS
GPIO 28	GPO	SEL_VID6	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPO	SEL_VID1 -	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	NEWCARD_OC#	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	LINKALERT#	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FANO_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FANO_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSTATUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM/+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	
-	-	-	
-	-	-	
-	-	-	

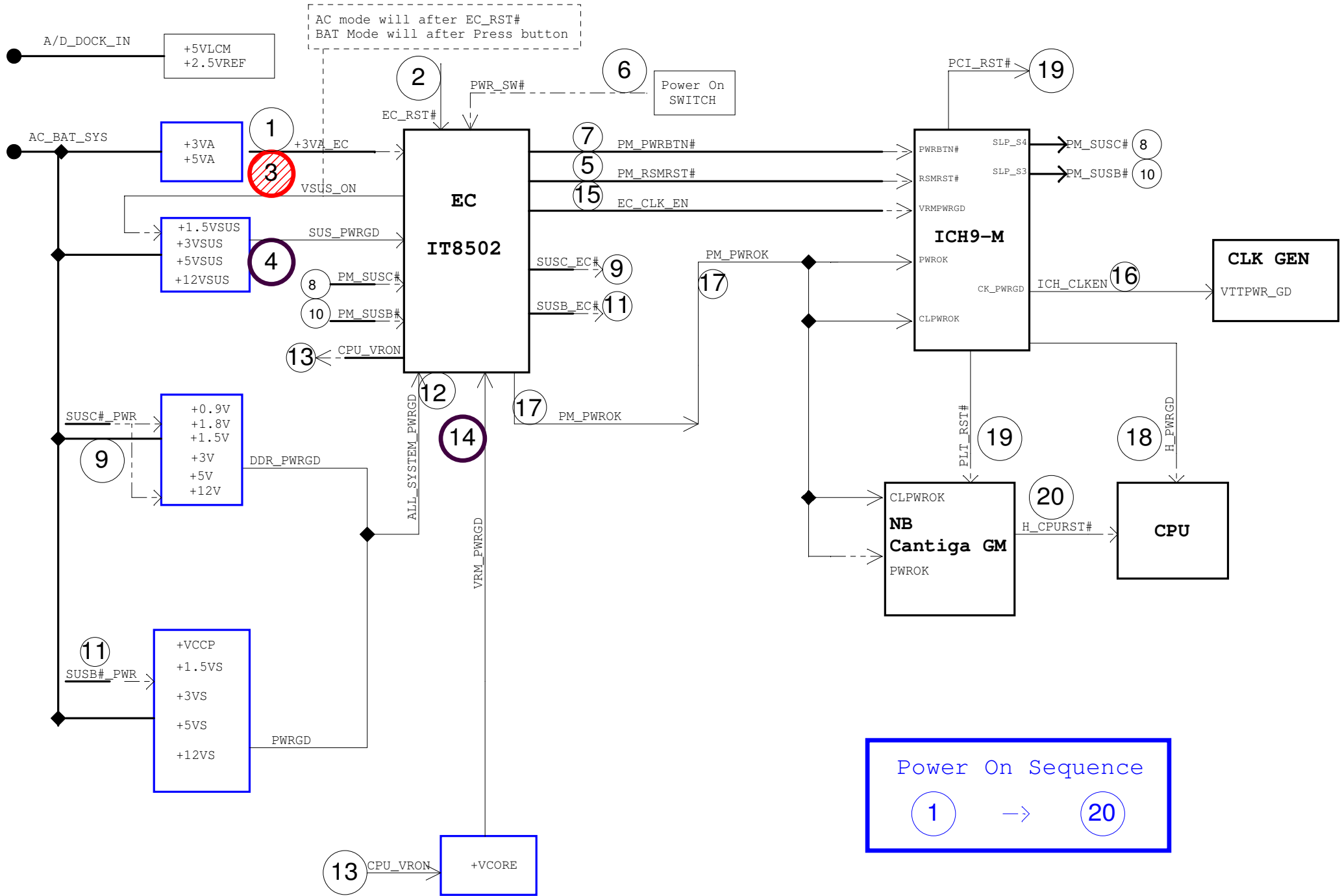
PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

PCIe Device	Bus	PCIe Device	Bus
Robson	PE(T/R)(p/n)1	3G/TV	PE(T/R)(p/n)4
WLAN	PE(T/R)(p/n)2	UWB	PE(T/R)(p/n)5
NEWCARD	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)6

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
CPU Thermal Sensor(MAX6619)	1001100x ( 98 )

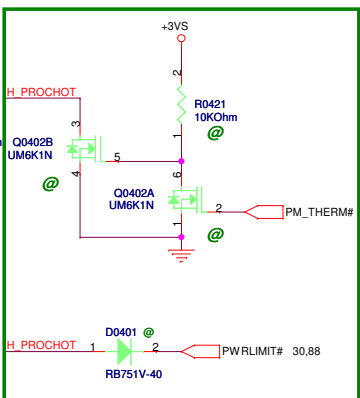
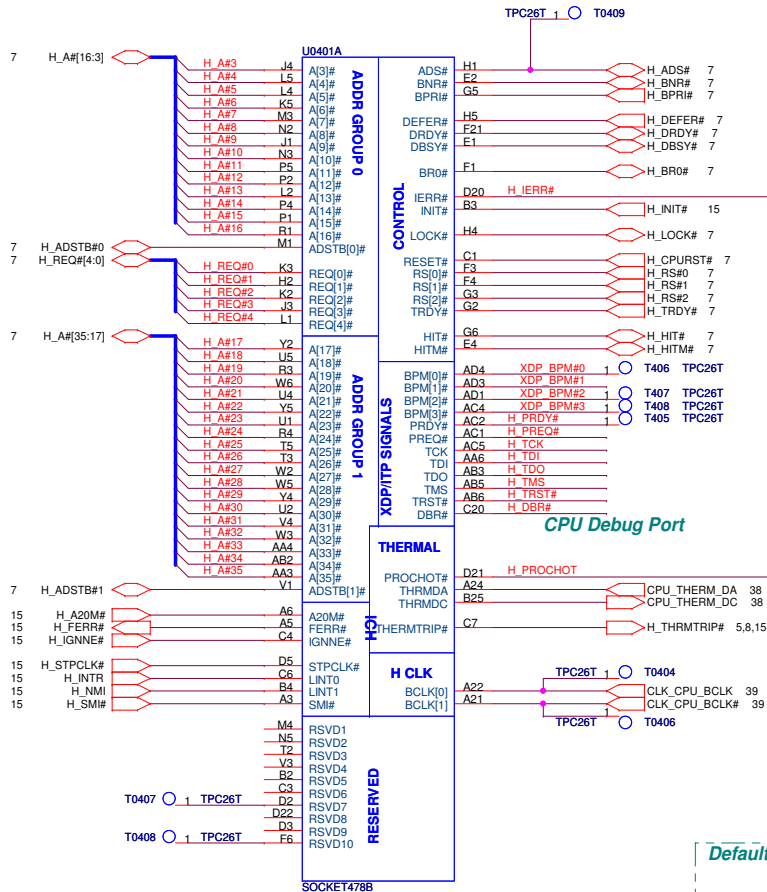
INT PU\*: PU or PD in special time  
 GPIO33 Internal Pull High, Go Low=Flash -  
 Descriptor Security will be overridden

ASUS		Title : System Setting
ASUSTek Computer INC. NB1		Engineer: Alex & Bruce
Size Custom	Project Name K401J/K501J	Rev 1.1
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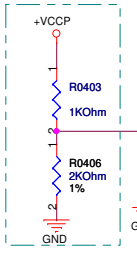


+VCCP +VCCP 5,7,8,9,11,12,15,18,39,42,82

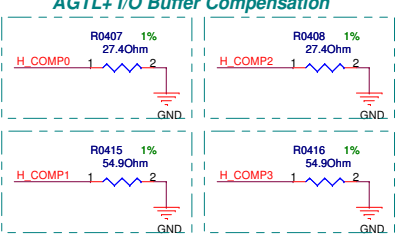
add test point



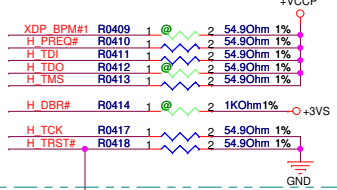
**AGTL+ I/O Voltage Reference**



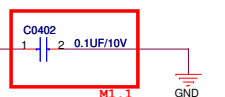
**AGTL+ I/O Buffer Compensation**



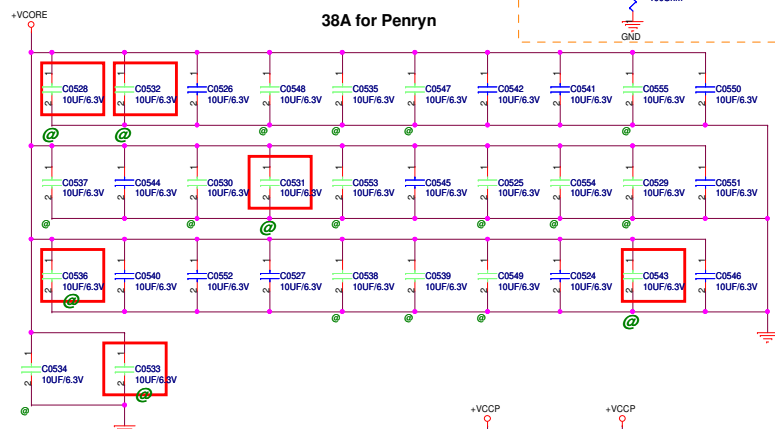
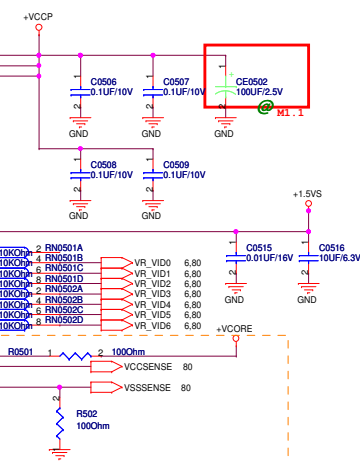
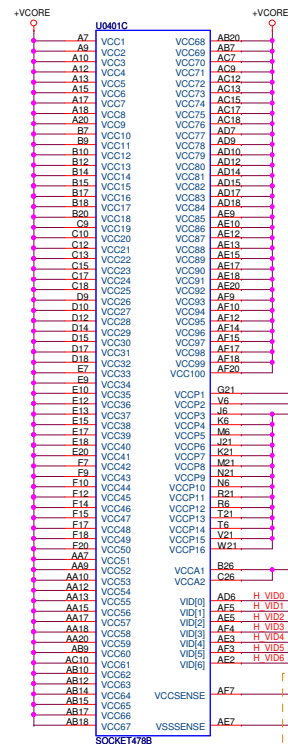
**Default Strapping When Not Used**



BCLK	FSB	BSEL	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1066	L	L	L

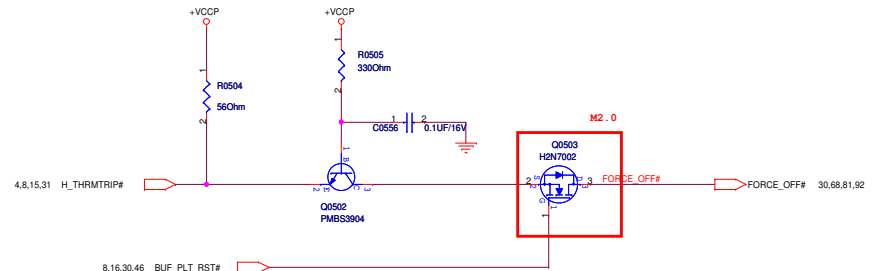


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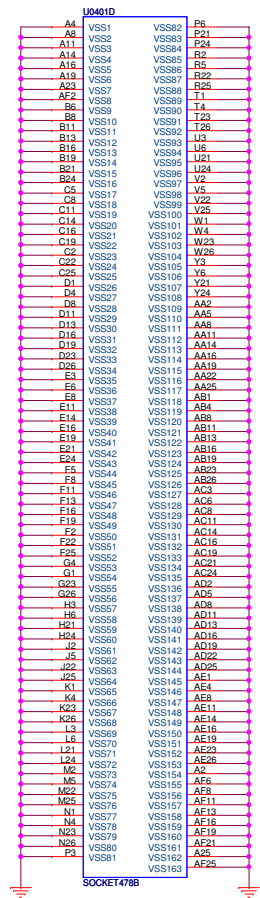


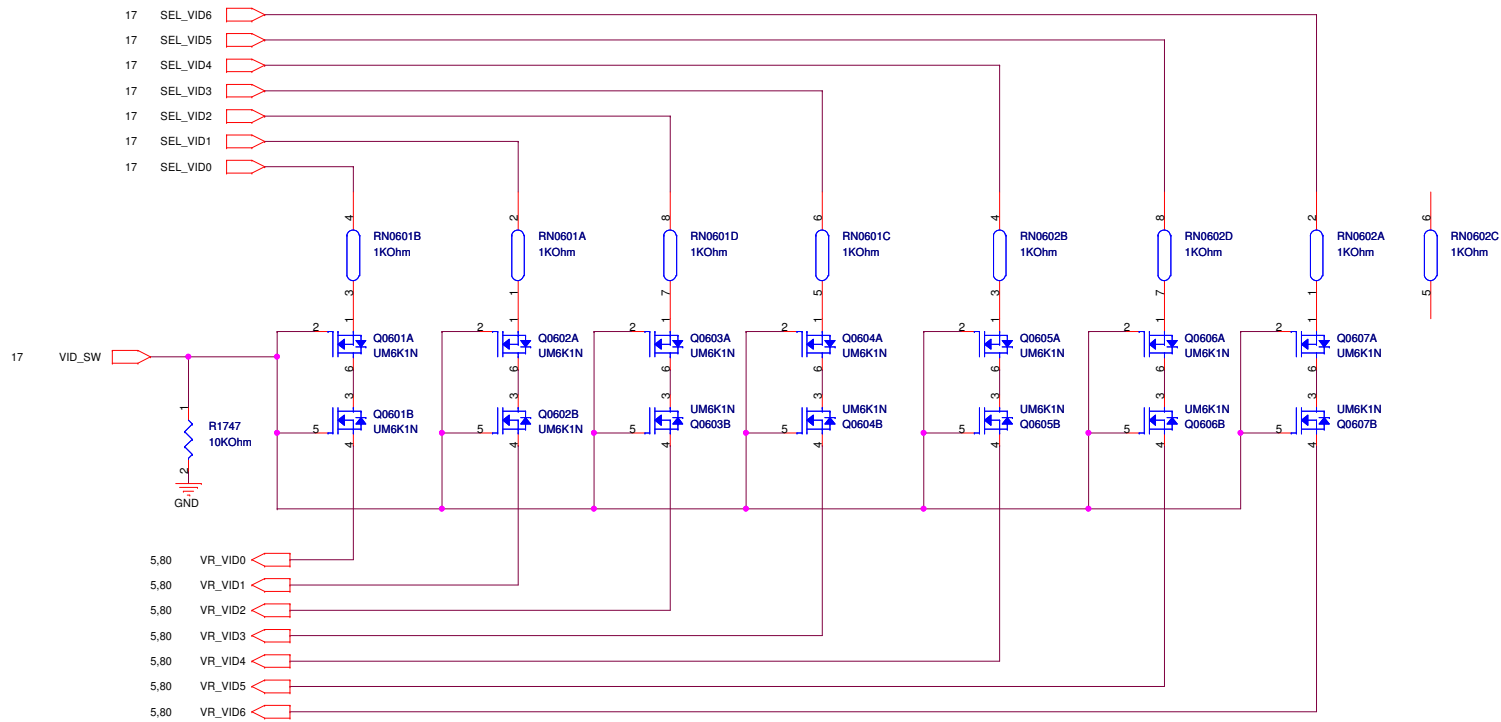
Decoupling guide from Intel

VCCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?



Thermal Trip signal (From CPU to ICH9-M and sequence)

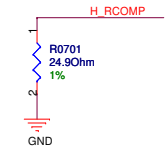




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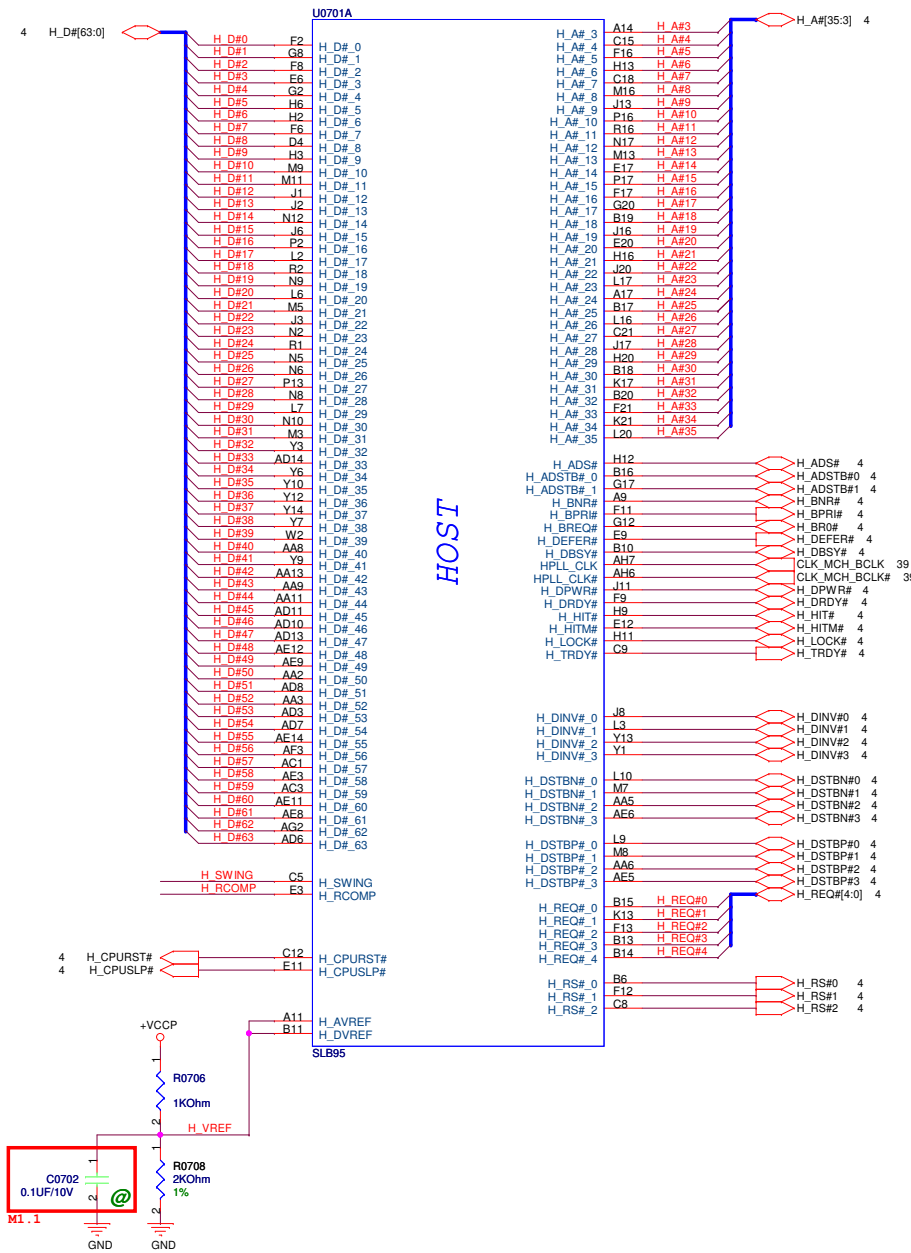
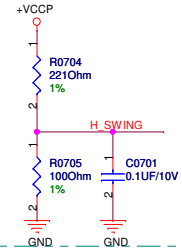
**RCOMP**

For Calibrating the FSB I/O Buffer

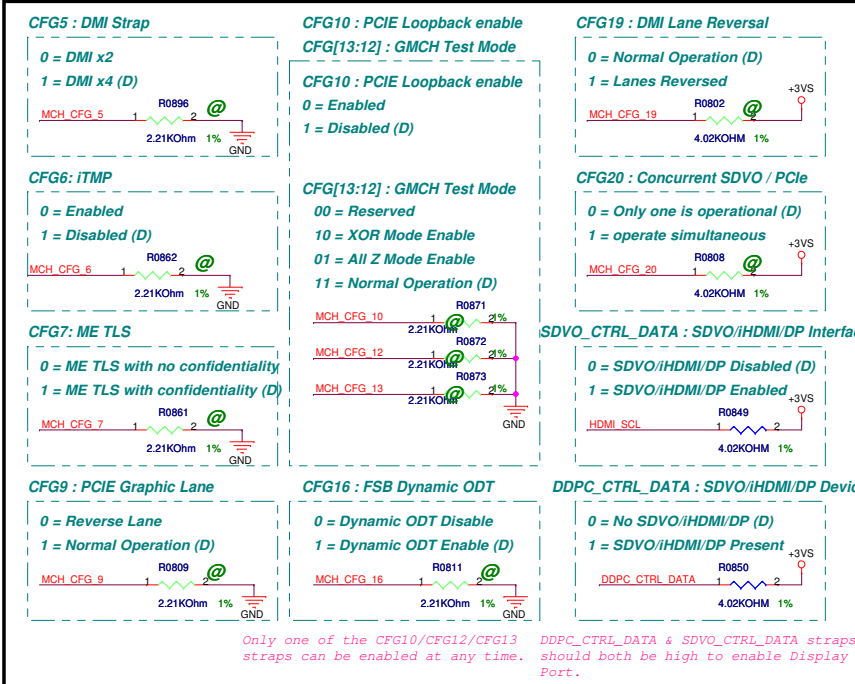


**Voltage Swing**

For Providing a Reference Voltage to The FSB RCOMP circuits



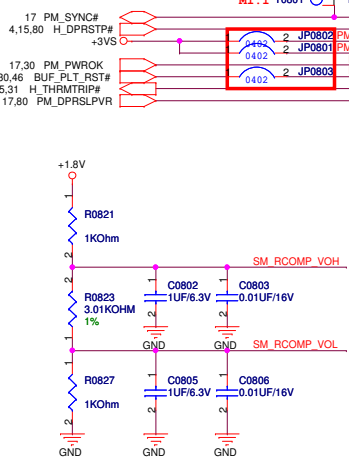
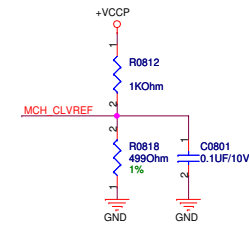
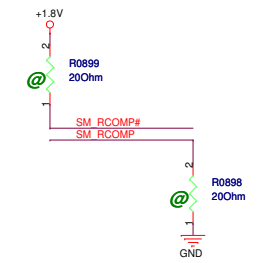
**GMCH Strapping**



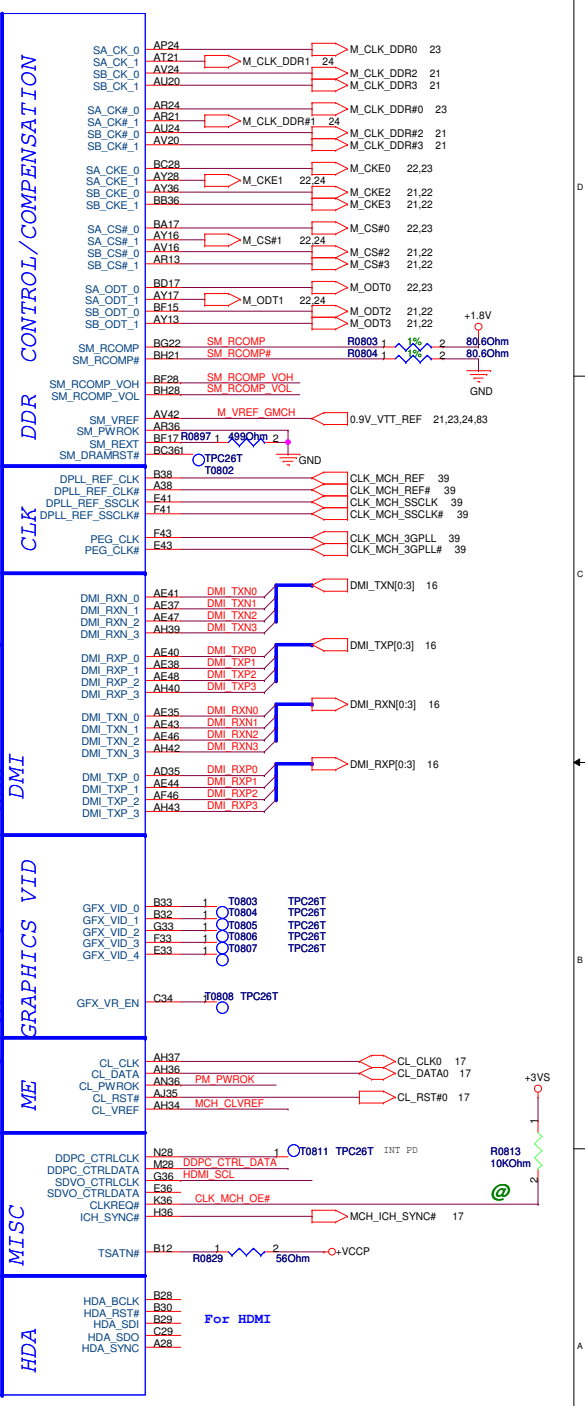
Only one of the CFG10/CFG12/CFG13 DDPC\_CTRL\_DATA & SDVO\_CTRL\_DATA straps should both be high to enable Display Port.

BCLK	FSB	BSEL2	BSEL1	BSEL0
266	1066	L	L	L
166	667	L	H	H
200	800	L	H	L

- 39 MCH\_BSEL0
- 39 MCH\_BSEL1
- 39 MCH\_BSEL2
- MCH\_CFG 5
- MCH\_CFG 6
- MCH\_CFG 7
- MCH\_CFG 9
- MCH\_CFG 10
- MCH\_CFG 12
- MCH\_CFG 13
- MCH\_CFG 16
- MCH\_CFG 19
- MCH\_CFG 20



- M36
- N36
- F33
- T33
- AH9
- AH10
- AH12
- AH13
- K12
- AL34
- AK34
- AN35
- AM35
- T24
- B31
- AJ6
- M1
- AY21
- A47
- BG23
- BF23
- BH18
- BF18
- RSVD1
- RSVD2
- RSVD3
- RSVD4
- RSVD5
- RSVD6
- RSVD7
- RSVD8
- ME\_JTAG\_TCK
- ME\_JTAG\_TDI
- ME\_JTAG\_TDO
- ME\_JTAG\_TMS
- RSVD11
- VSS
- RSVD13
- RSVD14
- NC
- RSVD16
- RSVD17
- RSVD18
- RSVD19
- NC\_1
- NC\_2
- NC\_3
- NC\_4
- NC\_5
- NC\_6
- NC\_7
- NC\_8
- NC\_9
- NC\_10
- NC\_11
- NC\_12
- NC\_13
- NC\_14
- NC\_15
- NC\_16
- NC\_17
- NC\_18
- NC\_19
- NC\_20
- NC\_21
- NC\_22
- NC\_23
- NC\_24
- NC\_25



<Variant Name>

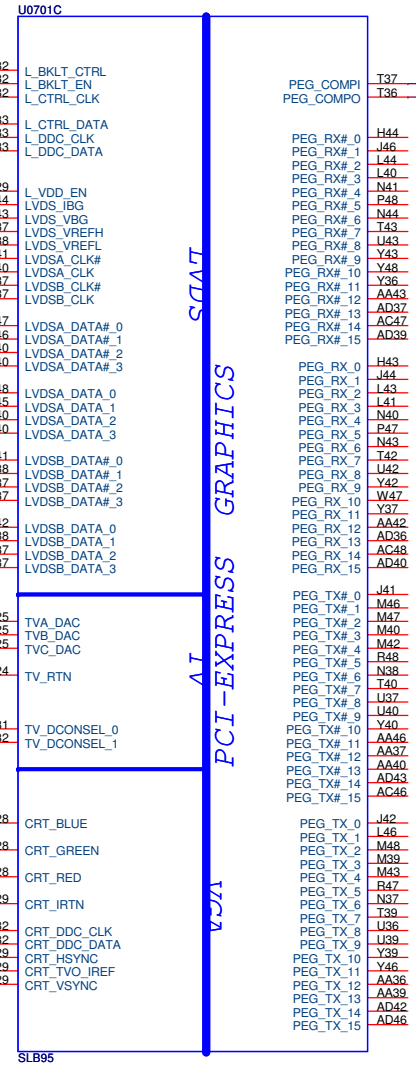
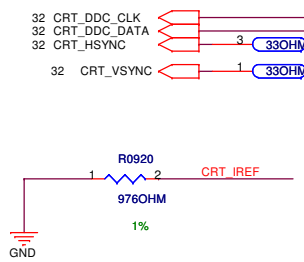
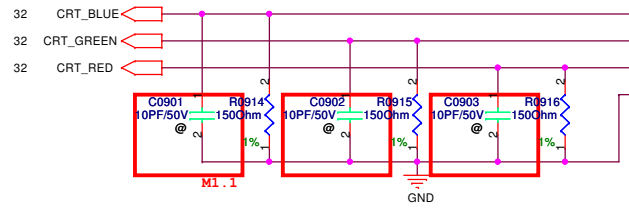
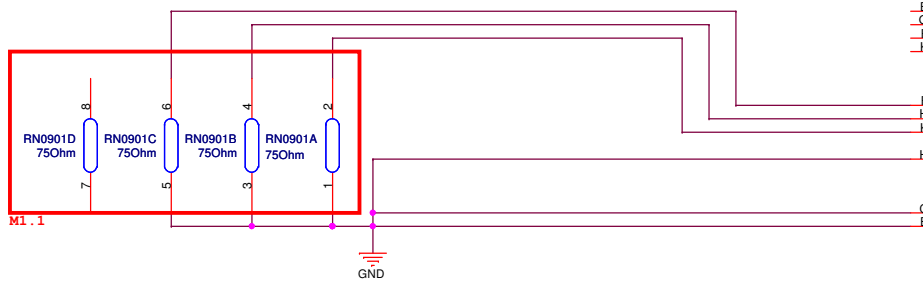
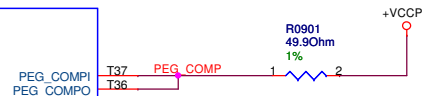
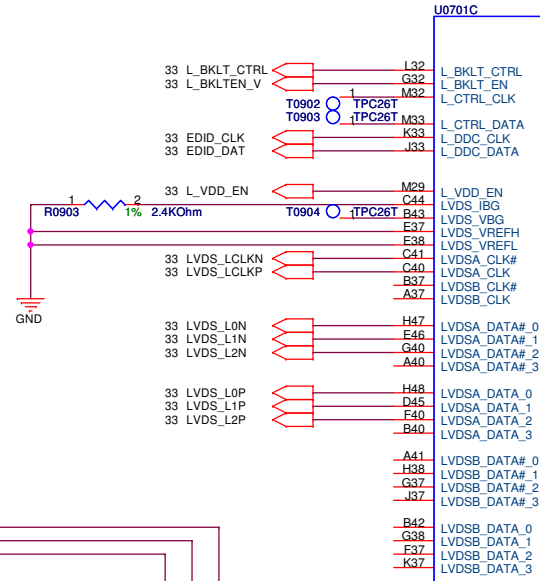
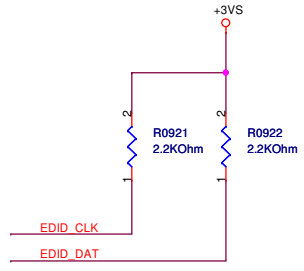
**ASUS** Title : NB-Cantiga(DMI & CFG)

ASUSTek COMPUTER INC. NB1 Engineer: N/A

Size	Project Name	Rev
Custom	<b>K401J / K501J</b>	1.1

Date: Monday, March 09, 2009 Sheet 8 of 96





LVDS AT PCI-EXPRESS GRAPHICS TVC

<Variant Name>

23,24 M\_A\_DQ[63:0]

M_A DQ0	AJ38	SA DO_0
M_A DQ1	AJ41	SA DO_1
M_A DQ2	AN38	SA DO_2
M_A DQ3	AM38	SA DO_3
M_A DQ4	AJ36	SA DO_4
M_A DQ5	AJ40	SA DO_5
M_A DQ6	AM44	SA DO_6
M_A DQ7	AM42	SA DO_7
M_A DQ8	AN43	SA DO_8
M_A DQ9	AN44	SA DO_9
M_A DQ10	AU40	SA DO_10
M_A DQ11	AT38	SA DO_11
M_A DQ12	AN41	SA DO_12
M_A DQ13	AN39	SA DO_13
M_A DQ14	AU44	SA DO_14
M_A DQ15	AU42	SA DO_15
M_A DQ16	AV39	SA DO_16
M_A DQ17	BA40	SA DO_17
M_A DQ18	BA40	SA DO_18
M_A DQ19	BD43	SA DO_19
M_A DQ20	AV41	SA DO_20
M_A DQ21	AY43	SA DO_21
M_A DQ22	BB41	SA DO_22
M_A DQ23	BC40	SA DO_23
M_A DQ24	AV37	SA DO_24
M_A DQ25	AV37	SA DO_25
M_A DQ26	AV37	SA DO_26
M_A DQ27	AT36	SA DO_27
M_A DQ28	AY38	SA DO_28
M_A DQ29	BB38	SA DO_29
M_A DQ30	AV36	SA DO_30
M_A DQ31	AV36	SA DO_31
M_A DQ32	BD13	SA DO_32
M_A DQ33	AI11	SA DO_33
M_A DQ34	BC11	SA DO_34
M_A DQ35	BA12	SA DO_35
M_A DQ36	AU13	SA DO_36
M_A DQ37	AV13	SA DO_37
M_A DQ38	BD12	SA DO_38
M_A DQ39	BC12	SA DO_39
M_A DQ40	BB9	SA DO_40
M_A DQ41	BA9	SA DO_41
M_A DQ42	AU10	SA DO_42
M_A DQ43	AV9	SA DO_43
M_A DQ44	BA11	SA DO_44
M_A DQ45	BD9	SA DO_45
M_A DQ46	AY8	SA DO_46
M_A DQ47	BA6	SA DO_47
M_A DQ48	AV5	SA DO_48
M_A DQ49	AV7	SA DO_49
M_A DQ50	AT9	SA DO_50
M_A DQ51	AN8	SA DO_51
M_A DQ52	AU5	SA DO_52
M_A DQ53	AU6	SA DO_53
M_A DQ54	AT5	SA DO_54
M_A DQ55	AN10	SA DO_55
M_A DQ56	AM11	SA DO_56
M_A DQ57	AM5	SA DO_57
M_A DQ58	AJ9	SA DO_58
M_A DQ59	AJ8	SA DO_59
M_A DQ60	AN12	SA DO_60
M_A DQ61	AM13	SA DO_61
M_A DQ62	AJ11	SA DO_62
M_A DQ63	AJ12	SA DO_63

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	22,23,24
SA_BS_1	BG18	M_A_BS1	22,23,24
SA_BS_2	AT25	M_A_BS2	22,23,24
SA_RAS#	BB20	M_A_RAS#	22,23,24
SA_CAS#	BD20	M_A_CAS#	22,23,24
SA_WE#	AY20	M_A_WE#	22,23,24
SA_DM_0	AM37	M_A_DM0	M_A_DM[7:0] 23,24
SA_DM_1	AT41	M_A_DM1	
SA_DM_2	AY41	M_A_DM2	
SA_DM_3	AU39	M_A_DM3	
SA_DM_4	BB12	M_A_DM4	
SA_DM_5	AY6	M_A_DM5	
SA_DM_6	AT7	M_A_DM6	
SA_DM_7	AJ5	M_A_DM7	
SA_DQS_0	AJ44	M_A_DQS0	M_A_DQS[7:0] 23,24
SA_DQS_1	AT44	M_A_DQS1	
SA_DQS_2	BA43	M_A_DQS2	
SA_DQS_3	BC37	M_A_DQS3	
SA_DQS_4	AW12	M_A_DQS4	
SA_DQS_5	BC4	M_A_DQS5	
SA_DQS_6	AJ8	M_A_DQS6	
SA_DQS_7	AM7	M_A_DQS7	
SA_DQS#_0	AJ43	M_A_DQS#0	M_A_DQS#[7:0] 23,24
SA_DQS#_1	AT43	M_A_DQS#1	
SA_DQS#_2	BA44	M_A_DQS#2	
SA_DQS#_3	BD37	M_A_DQS#3	
SA_DQS#_4	AY12	M_A_DQS#4	
SA_DQS#_5	BD8	M_A_DQS#5	
SA_DQS#_6	AJ9	M_A_DQS#6	
SA_DQS#_7	AM8	M_A_DQS#7	
SA_MA_0	BA21	M_A_A0	M_A_A[13:0] 22,23,24
SA_MA_1	BC24	M_A_A1	
SA_MA_2	BG24	M_A_A2	
SA_MA_3	BH24	M_A_A3	
SA_MA_4	BG25	M_A_A4	
SA_MA_5	BA24	M_A_A5	
SA_MA_6	BD24	M_A_A6	
SA_MA_7	BG27	M_A_A7	
SA_MA_8	BF25	M_A_A8	
SA_MA_9	AW24	M_A_A9	
SA_MA_10	BC21	M_A_A10	
SA_MA_11	BG26	M_A_A11	
SA_MA_12	BH26	M_A_A12	
SA_MA_13	BH17	M_A_A13	
SA_MA_14	AY25		

SLB95

21 M\_B\_DQ[63:0]

M_B DQ0	AK47	SB DO_0
M_B DQ1	AH46	SB DO_1
M_B DQ2	AP47	SB DO_2
M_B DQ3	AP46	SB DO_3
M_B DQ4	AJ46	SB DO_4
M_B DQ5	AM48	SB DO_5
M_B DQ6	AM48	SB DO_6
M_B DQ7	AP48	SB DO_7
M_B DQ8	AU47	SB DO_8
M_B DQ9	AU46	SB DO_9
M_B DQ10	BA48	SB DO_10
M_B DQ11	AY48	SB DO_11
M_B DQ12	AT47	SB DO_12
M_B DQ13	AR47	SB DO_13
M_B DQ14	BA47	SB DO_14
M_B DQ15	BC47	SB DO_15
M_B DQ16	BC46	SB DO_16
M_B DQ17	BC44	SB DO_17
M_B DQ18	BG43	SB DO_18
M_B DQ19	BF43	SB DO_19
M_B DQ20	BE45	SB DO_20
M_B DQ21	BC41	SB DO_21
M_B DQ22	BF40	SB DO_22
M_B DQ23	BF41	SB DO_23
M_B DQ24	BG38	SB DO_24
M_B DQ25	BF38	SB DO_25
M_B DQ26	BH35	SB DO_26
M_B DQ27	BG35	SB DO_27
M_B DQ28	BH40	SB DO_28
M_B DQ29	BG39	SB DO_29
M_B DQ30	BG34	SB DO_30
M_B DQ31	BH34	SB DO_31
M_B DQ32	BH14	SB DO_32
M_B DQ33	BG12	SB DO_33
M_B DQ34	BH11	SB DO_34
M_B DQ35	BG8	SB DO_35
M_B DQ36	BH12	SB DO_36
M_B DQ37	BF11	SB DO_37
M_B DQ38	BF8	SB DO_38
M_B DQ39	BG7	SB DO_39
M_B DQ40	BC5	SB DO_40
M_B DQ41	BC6	SB DO_41
M_B DQ42	AY3	SB DO_42
M_B DQ43	AY1	SB DO_43
M_B DQ44	BF6	SB DO_44
M_B DQ45	BF5	SB DO_45
M_B DQ46	BA1	SB DO_46
M_B DQ47	BD3	SB DO_47
M_B DQ48	AV2	SB DO_48
M_B DQ49	AU3	SB DO_49
M_B DQ50	AR3	SB DO_50
M_B DQ51	AN2	SB DO_51
M_B DQ52	AY2	SB DO_52
M_B DQ53	AV1	SB DO_53
M_B DQ54	AP3	SB DO_54
M_B DQ55	AR1	SB DO_55
M_B DQ56	AL1	SB DO_56
M_B DQ57	AL2	SB DO_57
M_B DQ58	AJ1	SB DO_58
M_B DQ59	AH1	SB DO_59
M_B DQ60	AM2	SB DO_60
M_B DQ61	AM3	SB DO_61
M_B DQ62	AH3	SB DO_62
M_B DQ63	AJ3	SB DO_63

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0	21,22
SB_BS_1	BB17	M_B_BS1	21,22
SB_BS_2	BB33	M_B_BS2	21,22
SB_RAS#	AU17	M_B_RAS#	21,22
SB_CAS#	BG16	M_B_CAS#	21,22
SB_WE#	BE14	M_B_WE#	21,22
SB_DM_0	AM47	M_B_DM0	M_B_DM[7:0] 21
SB_DM_1	AY47	M_B_DM1	
SB_DM_2	BD40	M_B_DM2	
SB_DM_3	BF35	M_B_DM3	
SB_DM_4	BG11	M_B_DM4	
SB_DM_5	BA3	M_B_DM5	
SB_DM_6	AP1	M_B_DM6	
SB_DM_7	AK2	M_B_DM7	
SB_DQS_0	AL47	M_B_DQS0	M_B_DQS[7:0] 21
SB_DQS_1	AV48	M_B_DQS1	
SB_DQS_2	BG41	M_B_DQS2	
SB_DQS_3	BG37	M_B_DQS3	
SB_DQS_4	BH9	M_B_DQS4	
SB_DQS_5	BB2	M_B_DQS5	
SB_DQS_6	AU1	M_B_DQS6	
SB_DQS_7	AN6	M_B_DQS7	
SB_DQS#_0	AL46	M_B_DQS#0	M_B_DQS#[7:0] 21
SB_DQS#_1	AV47	M_B_DQS#1	
SB_DQS#_2	BH41	M_B_DQS#2	
SB_DQS#_3	BH37	M_B_DQS#3	
SB_DQS#_4	BG9	M_B_DQS#4	
SB_DQS#_5	BC2	M_B_DQS#5	
SB_DQS#_6	AT2	M_B_DQS#6	
SB_DQS#_7	AN5	M_B_DQS#7	
SB_MA_0	AV17	M_B_A0	M_B_A[14:0] 21,22
SB_MA_1	BA25	M_B_A1	
SB_MA_2	BC25	M_B_A2	
SB_MA_3	AU25	M_B_A3	
SB_MA_4	AW25	M_B_A4	
SB_MA_5	BE28	M_B_A5	
SB_MA_6	AU28	M_B_A6	
SB_MA_7	AW28	M_B_A7	
SB_MA_8	AT33	M_B_A8	
SB_MA_9	BD33	M_B_A9	
SB_MA_10	BB16	M_B_A10	
SB_MA_11	AW33	M_B_A11	
SB_MA_12	AY33	M_B_A12	
SB_MA_13	BH15	M_B_A13	
SB_MA_14	AU33	M_B_A14	

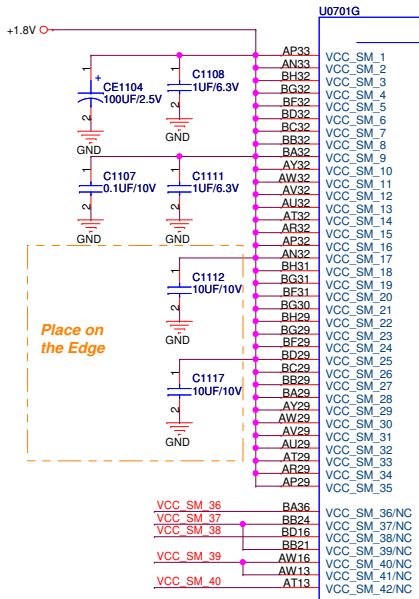
SLB95

<Variant Name>

**ASUS** Title : NB-Cantiga(DDR2)  
 ASUSTeK COMPUTER INC. NB1 Engineer: N/A

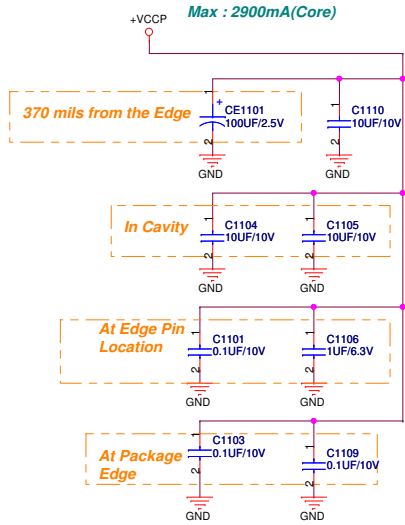
Size	Project Name	Rev
Custom	K401J/K501J	1.1
Date: Monday, March 09, 2009	Sheet 10 of 96	

Max : 3000mA(DDR2)



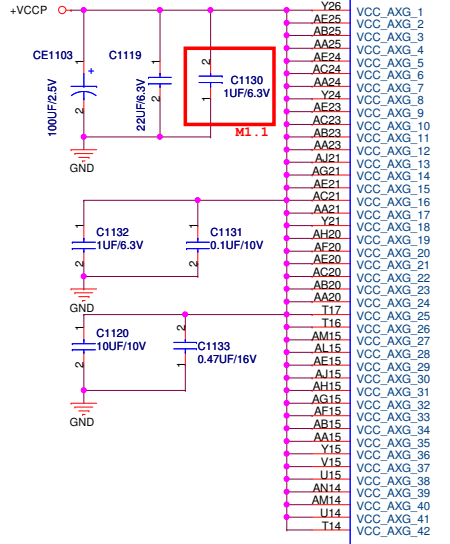
VCC SM POWER

(Graph Core)



VCC CORE POWER

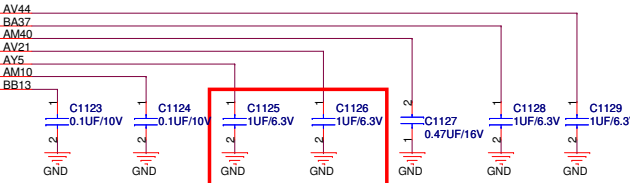
Max : 8700mA(Graphic Core)



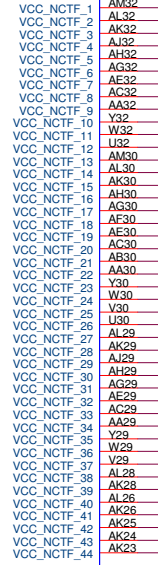
VCC GFX NCTF

Route VCC\_AXG\_SENSE and VSS\_AXG\_SENSE differentially.

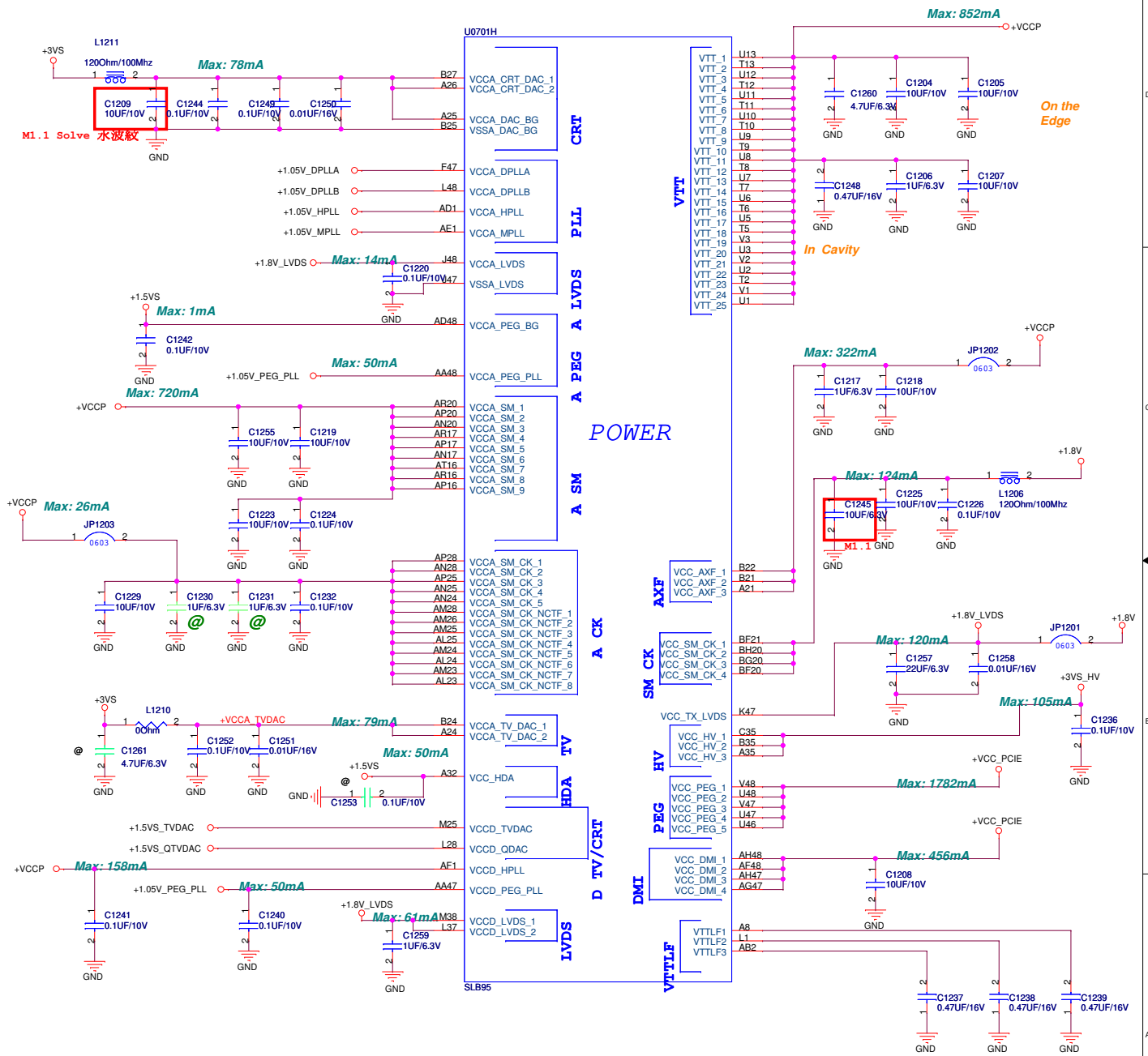
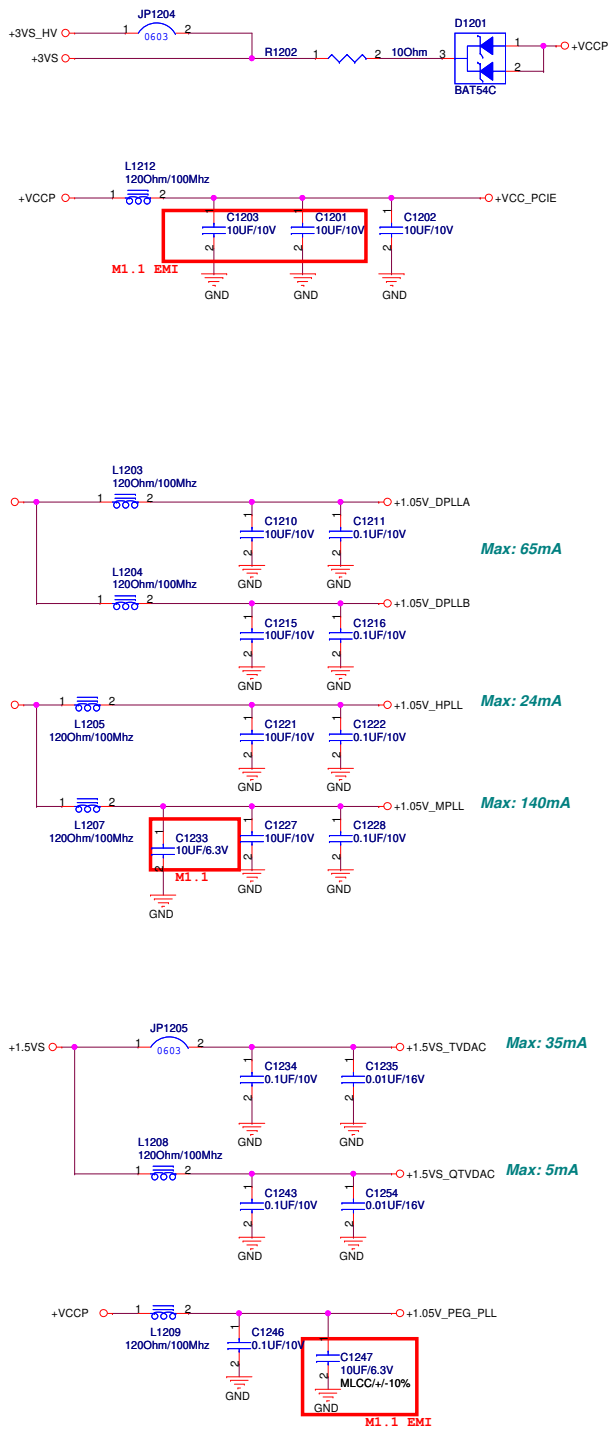
VCC SM LF

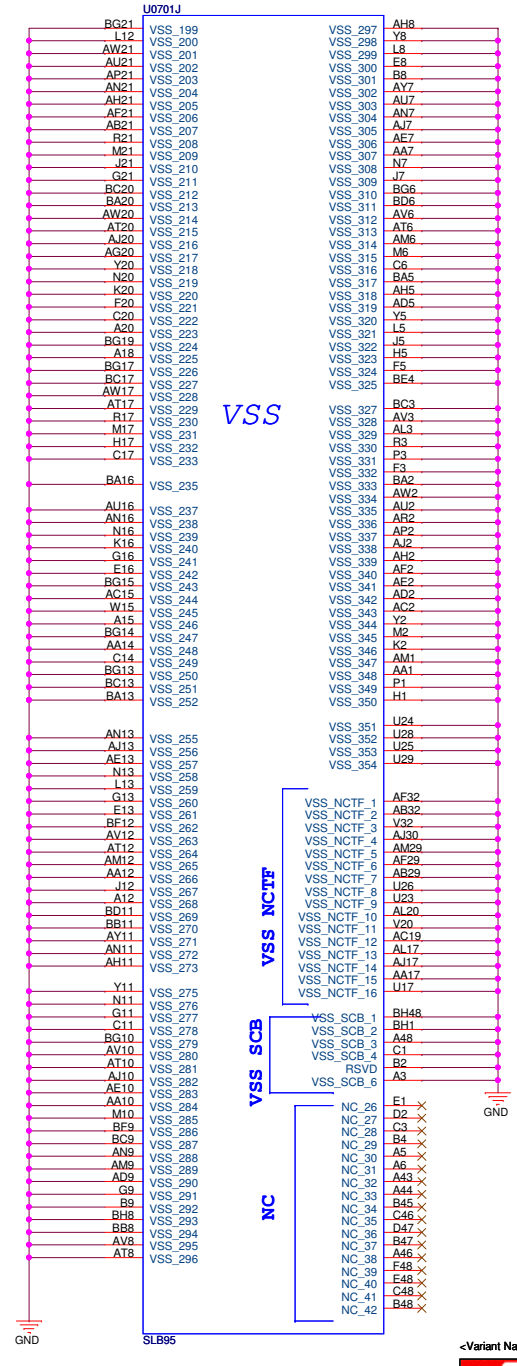
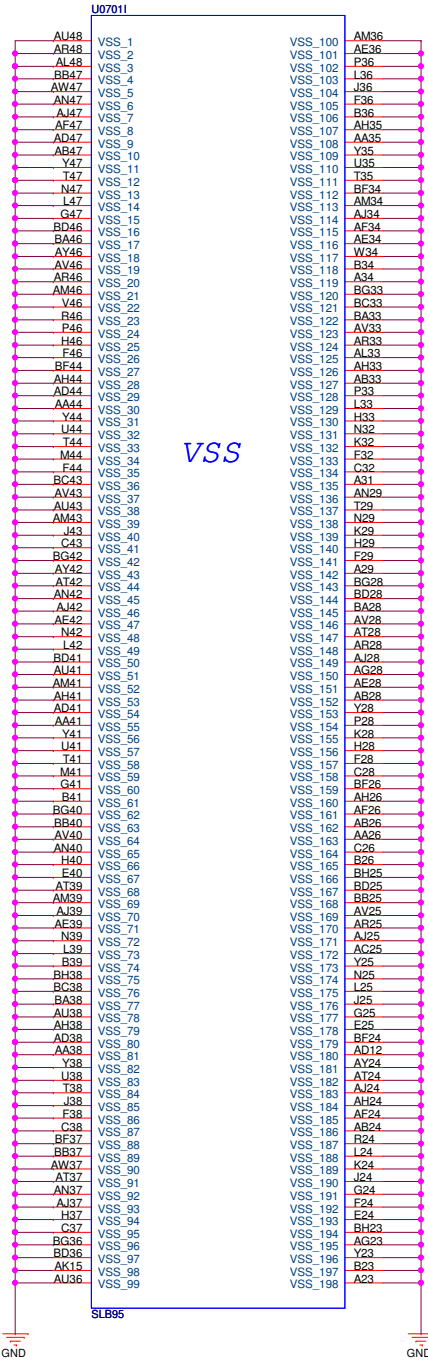


VCC NCTF




ASUS Title : NB\_Cantiga(PWR)  
 ASUSTek COMPUTER INC. NB1 Engineer: N/A  
 Size Project Name  
 Custom K40IJ/K50IJ Rev 1.1  
 Date: Monday, March 09, 2009 Sheet 11 of 96





<Variant Name>



Title : NB\_Cantiga(GND)

ASUSTek COMPUTER INC. NB1 Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009 Sheet 13 of 96

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		<b>Title :</b> Schematic page name
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A
Size	Project Name	Rev
C	<b>K40LJ/K50LJ</b>	1.1
Date: Monday, March 09, 2009		Sheet 14 of 95

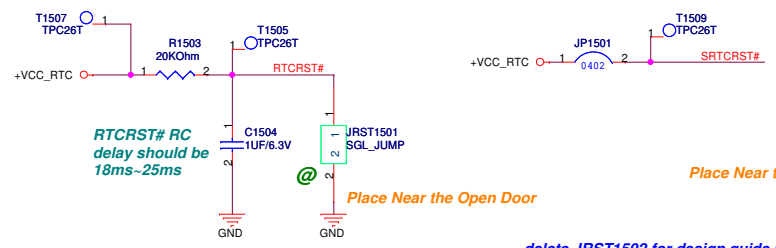
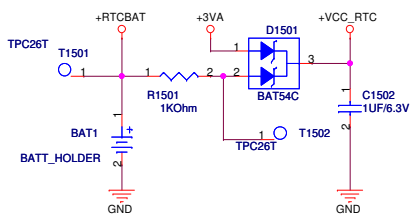
5

4

3

2

1

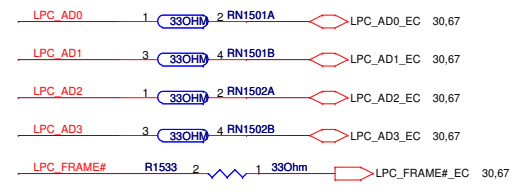


**RTC RST# RC delay should be 18ms-25ms**

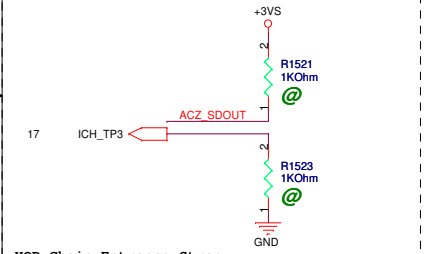
**Place Near the Open Door**

**Place Near the Open Door**

**delete JRST1502 for design guide recommendation.**

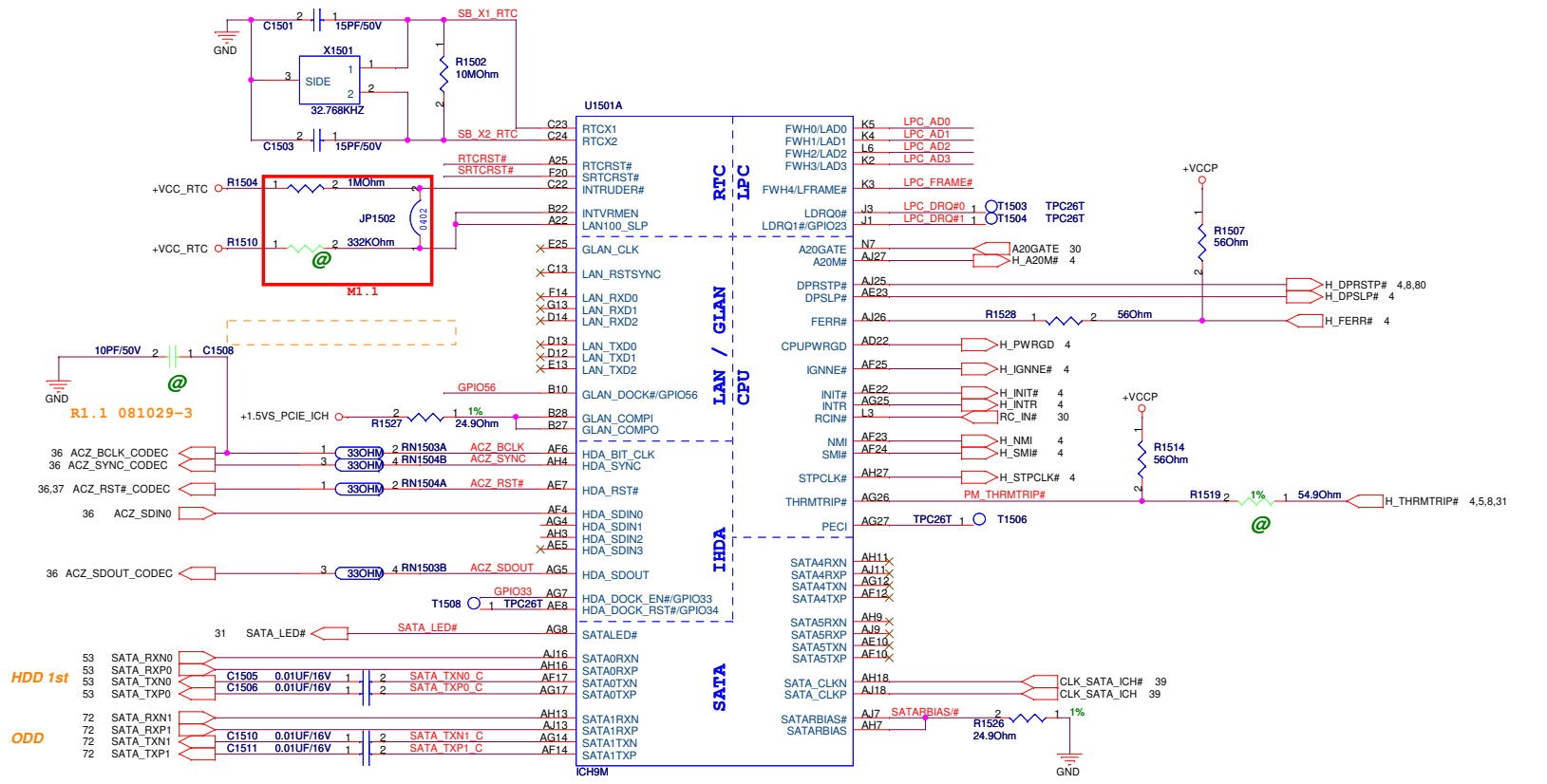
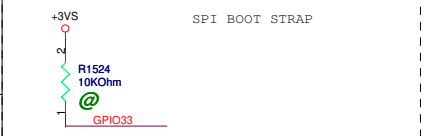


ICH\_INTVRMEN(VCCSUS1\_05, VCCSUS1\_5, VCCCL1\_5)  
 Low - Disabled Internal VR  
 High - Enable Internal VR(D)  
 ICH\_LAN100(VCCLAN1\_05, VCCCL1\_05)  
 Low - Disabled Internal VR  
 High - Enable Internal VR(D)



**XOR Chain Entrance Strap**

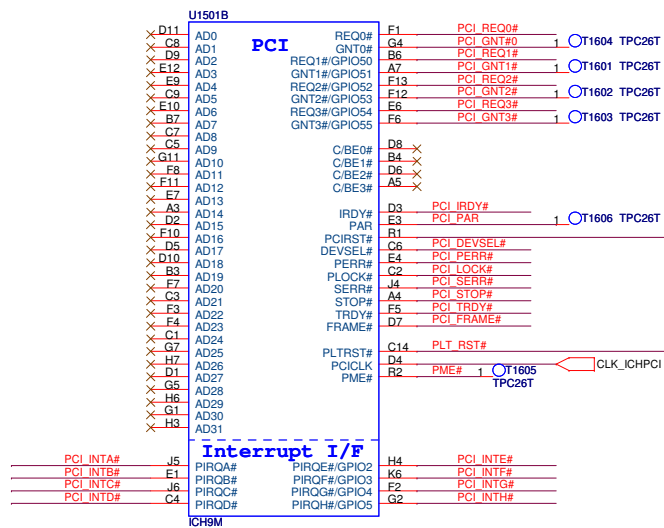
ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (D)
1	1	Set PCIe port config bit 1



**HDD 1st**

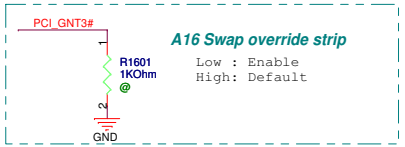
**ODD**





**ICH8 Boot BIOS Select**

	GNT#0	CS#1
LPC	H	H
PCI	H	L
SPI	L	H



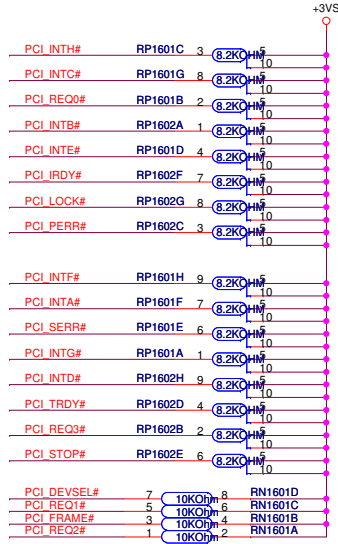
**Buffer to Reduce Loading on PLT\_RST#**

JP1601

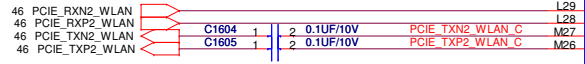
R1604 1KOhm

BUF\_PLT\_RST# 5,8,30,46

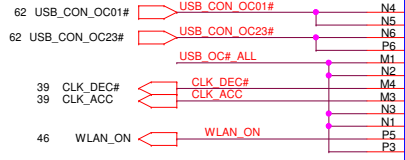
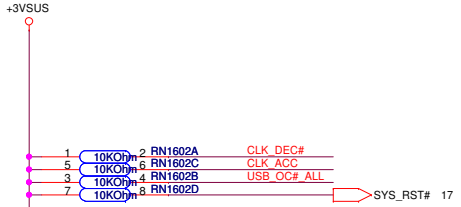
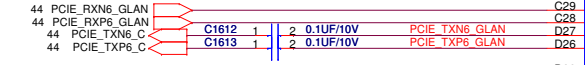
GND



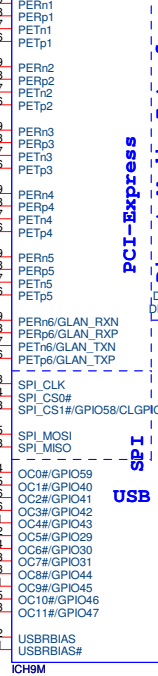
**WLAN**



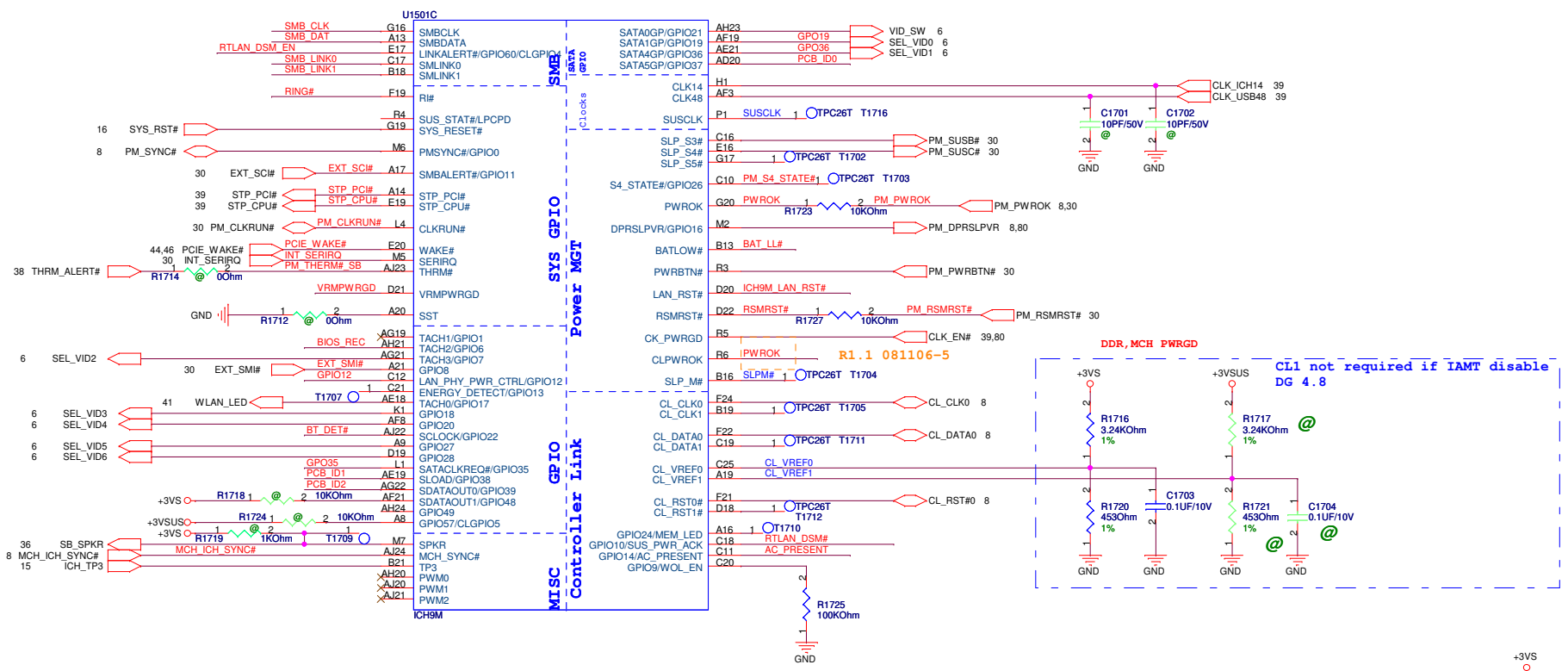
**GLAN**



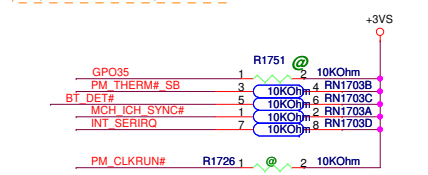
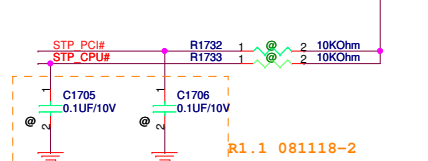
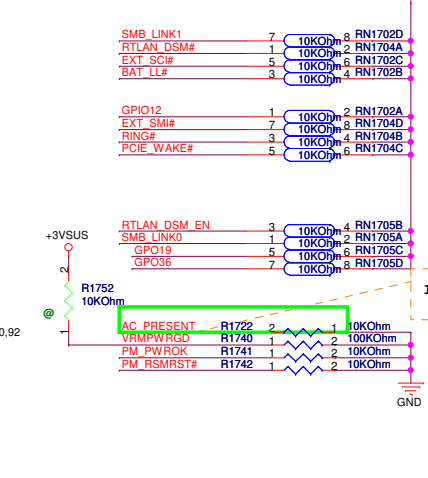
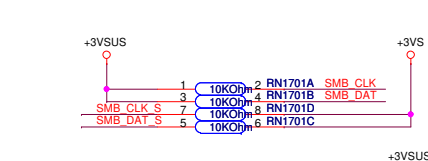
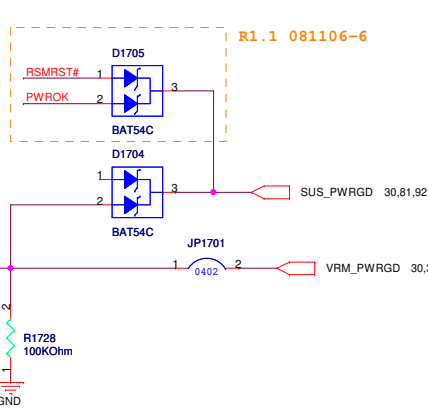
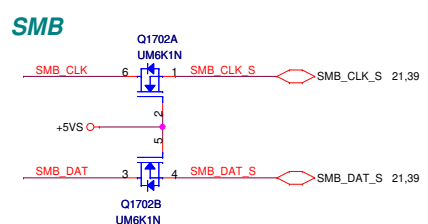
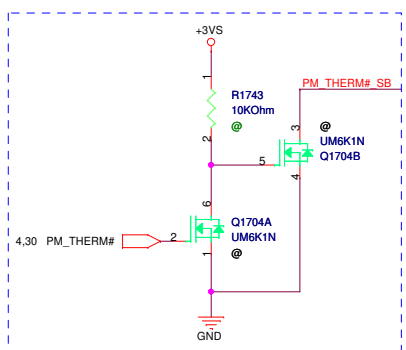
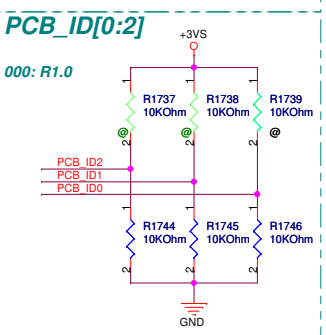
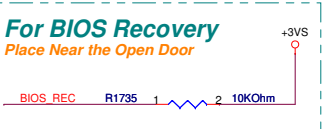
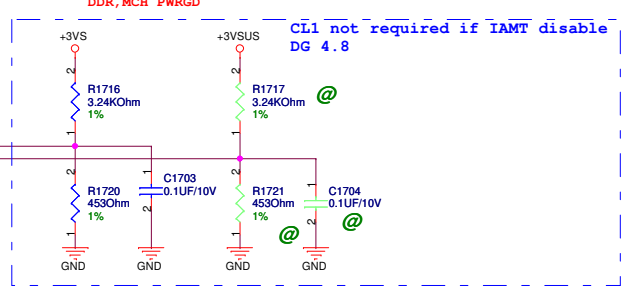
**U1501D**



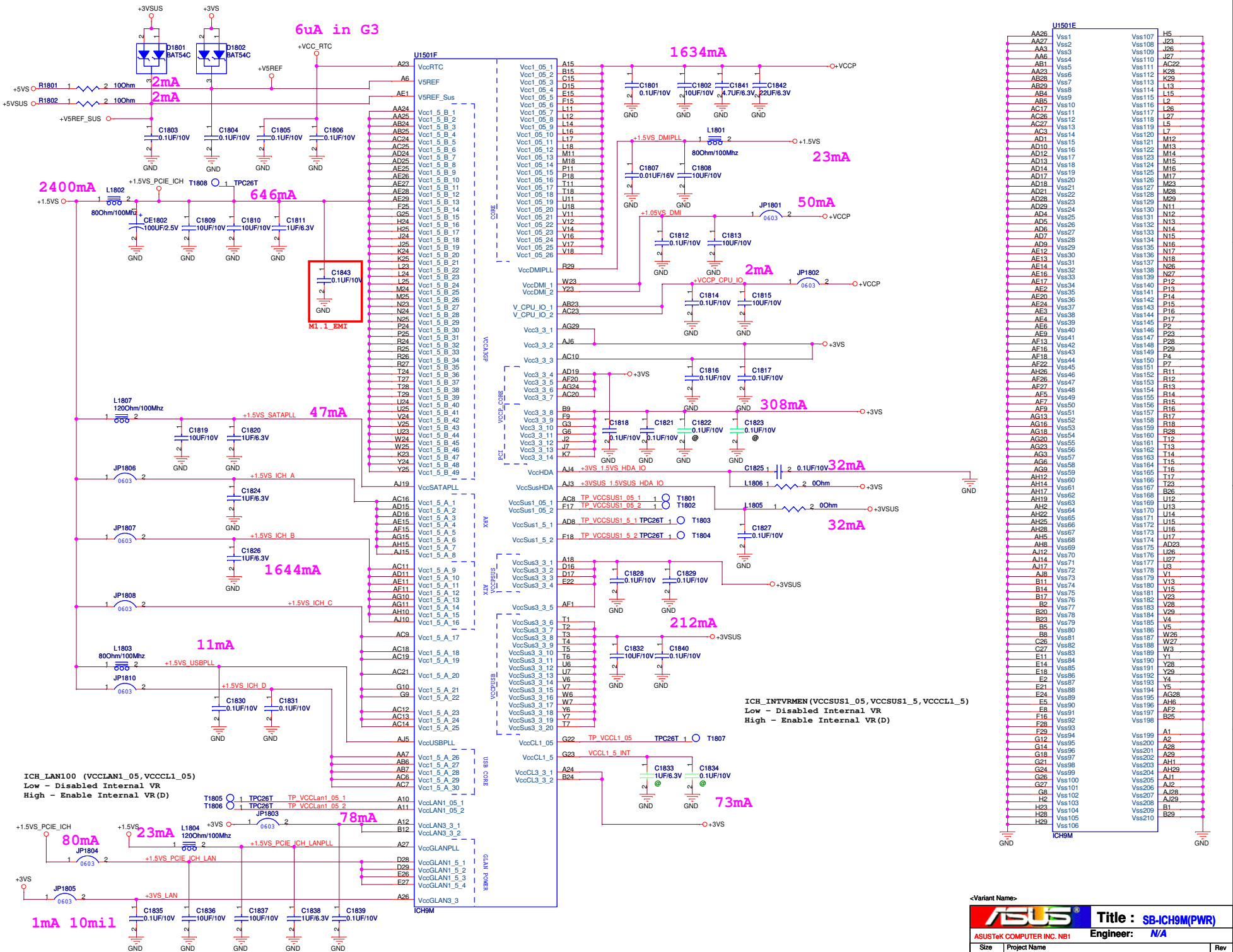




No Reboot Strap  
 Low = Default  
 High = No Reboot



**ASUS** Title : SB-ICH9M(3)  
 ASUSTek COMPUTER INC. NBI Engineer: N/A  
 Size Project Name  
 Custom K40IJ/K50IJ  
 Date: Monday, March 09, 2009 Sheet 17 of 96



AA26	Vss1	Vss107	H5
AA27	Vss2	Vss108	J26
AA3	Vss3	Vss109	J27
AA6	Vss4	Vss110	J27
AB1	Vss5	Vss111	AC22
AB2	Vss6	Vss112	K29
AB23	Vss7	Vss113	L13
AB29	Vss8	Vss114	L2
AB4	Vss9	Vss115	L15
AB5	Vss10	Vss116	L26
AC17	Vss11	Vss117	L27
AC26	Vss12	Vss118	L5
AC27	Vss13	Vss119	L7
AC3	Vss14	Vss120	M12
AD1	Vss15	Vss121	M13
AD10	Vss16	Vss122	M14
AD12	Vss17	Vss123	M15
AD13	Vss18	Vss124	M16
AD14	Vss19	Vss125	M17
AD18	Vss20	Vss126	M23
AD21	Vss21	Vss127	M28
AD22	Vss22	Vss128	M29
AD29	Vss23	Vss129	N11
AD4	Vss24	Vss130	N11
AD5	Vss25	Vss131	N12
AD6	Vss26	Vss132	N13
AD7	Vss27	Vss133	N14
AD9	Vss28	Vss134	N15
AE12	Vss29	Vss135	N16
AE13	Vss30	Vss136	N18
AE14	Vss31	Vss137	N26
AE15	Vss32	Vss138	P12
AE16	Vss33	Vss139	N27
AE17	Vss34	Vss140	P13
AE20	Vss35	Vss141	P14
AE24	Vss36	Vss142	P15
AE3	Vss37	Vss143	P16
AE4	Vss38	Vss144	P17
AE6	Vss39	Vss145	P2
AE9	Vss40	Vss146	P28
AE11	Vss41	Vss147	P23
AE16	Vss42	Vss148	P29
AE18	Vss43	Vss149	P4
AF18	Vss44	Vss150	P4
AF22	Vss45	Vss151	R11
AH26	Vss46	Vss152	R12
AF26	Vss47	Vss153	R13
AF27	Vss48	Vss154	R14
AE5	Vss49	Vss155	R14
AF7	Vss50	Vss156	R16
AF9	Vss51	Vss157	R17
AG13	Vss52	Vss158	R18
AG16	Vss53	Vss159	R23
AG18	Vss54	Vss160	T12
AG20	Vss55	Vss161	T13
AG23	Vss56	Vss162	T15
AG3	Vss57	Vss163	T14
AG6	Vss58	Vss164	T16
AG9	Vss59	Vss165	T17
AH12	Vss60	Vss166	T23
AH14	Vss61	Vss167	B26
AH17	Vss62	Vss168	H12
AH19	Vss63	Vss169	H13
AH2	Vss64	Vss170	V13
AH22	Vss65	Vss171	H14
AH25	Vss66	Vss172	H15
AH28	Vss67	Vss173	H16
AH5	Vss68	Vss174	H17
AH8	Vss69	Vss175	AD23
AH12	Vss70	Vss176	U26
AH14	Vss71	Vss177	U27
AH17	Vss72	Vss178	U3
AH8	Vss73	Vss179	V13
B11	Vss74	Vss180	V15
B17	Vss75	Vss181	V23
B2	Vss76	Vss182	V28
B20	Vss77	Vss183	V29
B23	Vss78	Vss184	V4
B5	Vss79	Vss185	V5
B5	Vss80	Vss186	W26
B8	Vss81	Vss187	W27
C26	Vss82	Vss188	W3
C27	Vss83	Vss189	Y1
E11	Vss84	Vss190	Y2
E14	Vss85	Vss191	Y28
E18	Vss86	Vss192	Y4
E2	Vss87	Vss193	Y5
E21	Vss88	Vss194	Y5
E24	Vss89	Vss195	AC28
E5	Vss90	Vss196	AH6
EA	Vss91	Vss197	AF2
F16	Vss92	Vss198	B25
F28	Vss93	Vss199	A1
F29	Vss94	Vss200	A2
G12	Vss95	Vss201	A28
G14	Vss96	Vss202	A29
G21	Vss97	Vss203	AH1
G24	Vss98	Vss204	AH20
G26	Vss99	Vss205	A11
G27	Vss100	Vss206	A12
G3	Vss101	Vss207	A22
H2	Vss102	Vss208	A23
H23	Vss103	Vss209	B1
H23	Vss104	Vss210	B29
H28	Vss105	Vss210	
H29	Vss106	Vss210	

ICH\_INTVRMEN (VCCSUS1\_05, VCCSUS1\_5, VCCCL1\_5)  
 Low - Disabled Internal VR  
 High - Enable Internal VR (D)

<Variant Name>

<b>ASUS</b>		<b>Title : SB-ICH9M(PWR)</b>
ASUSTek COMPUTER INC. NB1		<b>Engineer: N/A</b>
Size	Project Name	Rev
Custom	<b>K40LI/K50IJ</b>	1.1
Date: Monday, March 08, 2009	Sheet	18 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	19 of 96

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<Variant Name>



ASUSTeK COMPUTER INC. NB1 **Engineer: N/A**

Size	Project Name	Rev
A3	<b>K40IJ/K50IJ</b>	1.1

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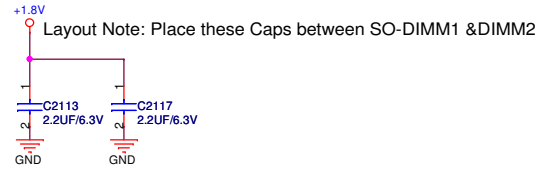
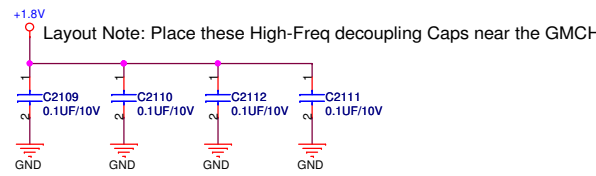
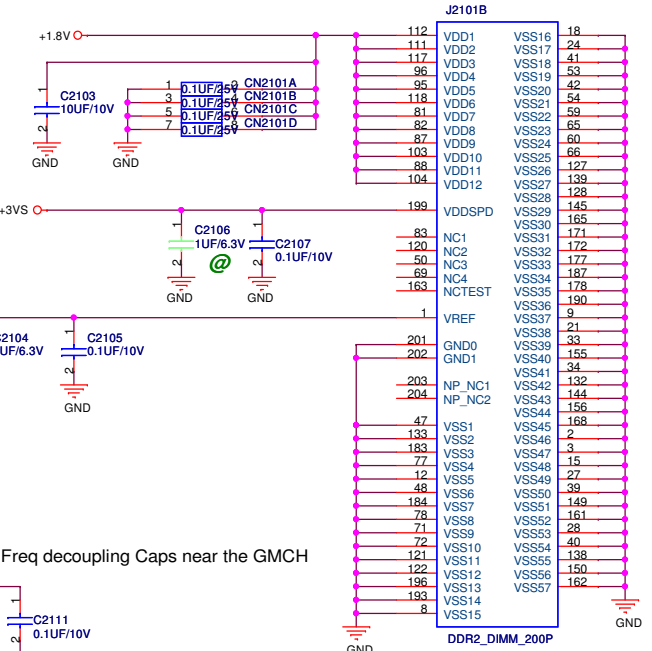
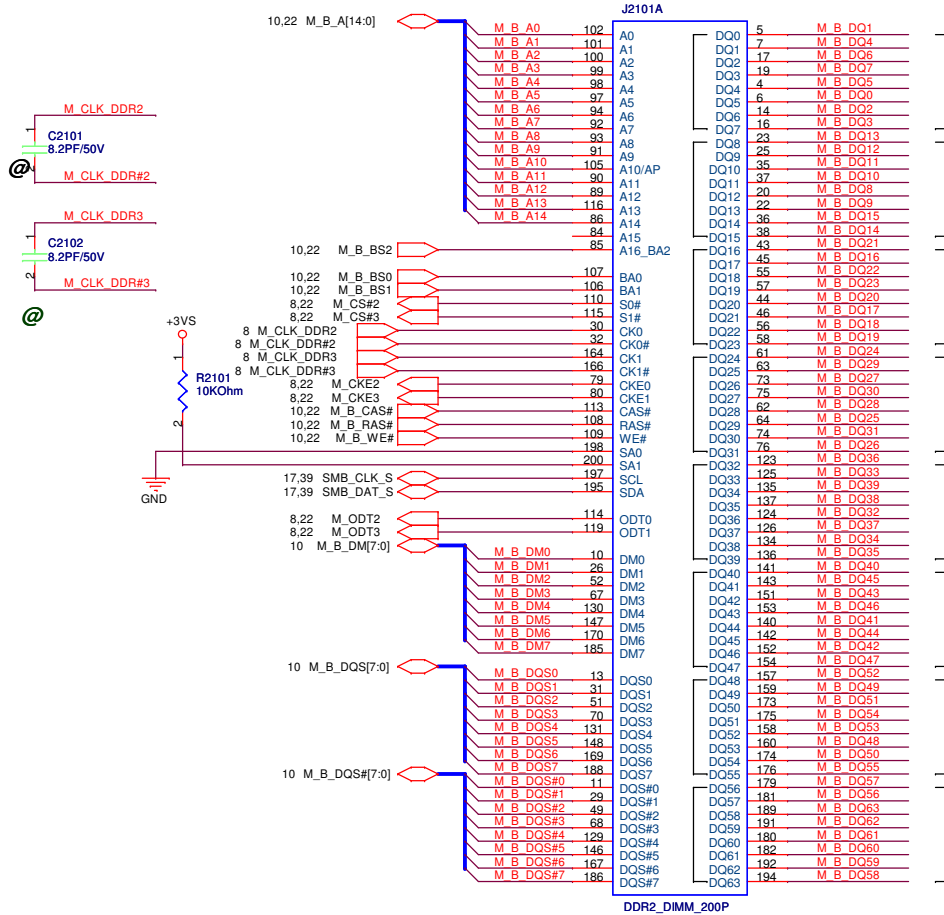
3

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# DDR2 200P H=9.2mm (Reverse Type)

M\_B\_DQ[63:0] 10



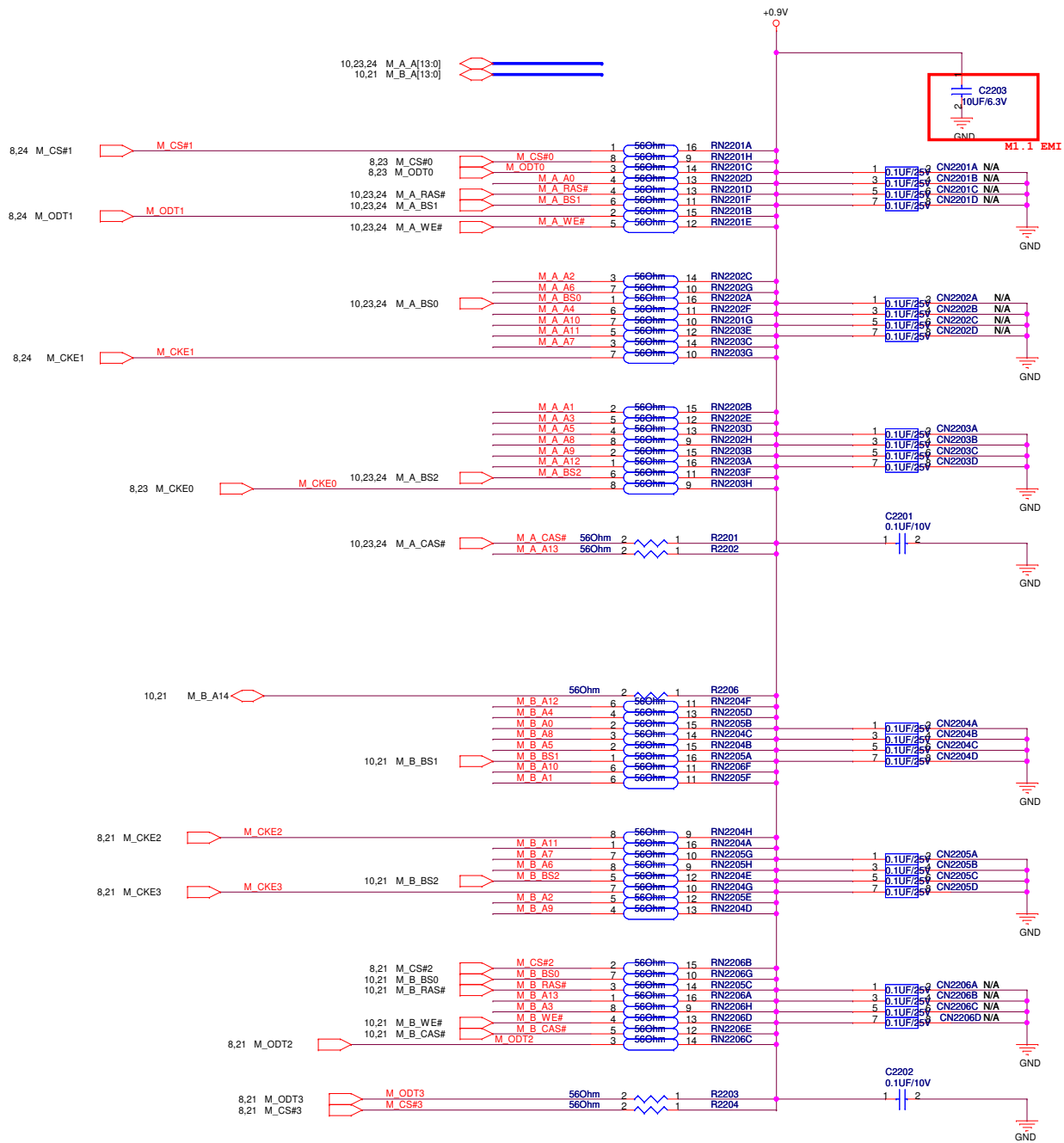
<Variant Name>

**ASUS** Title: **DDR2 SO-DIMM1**

ASUSTeK COMPUTER INC. NB1 Engineer: **N/A**

Size	Project Name	Rev
Custom	<b>K401J/K501J</b>	1.1

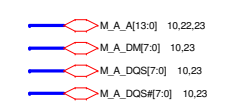
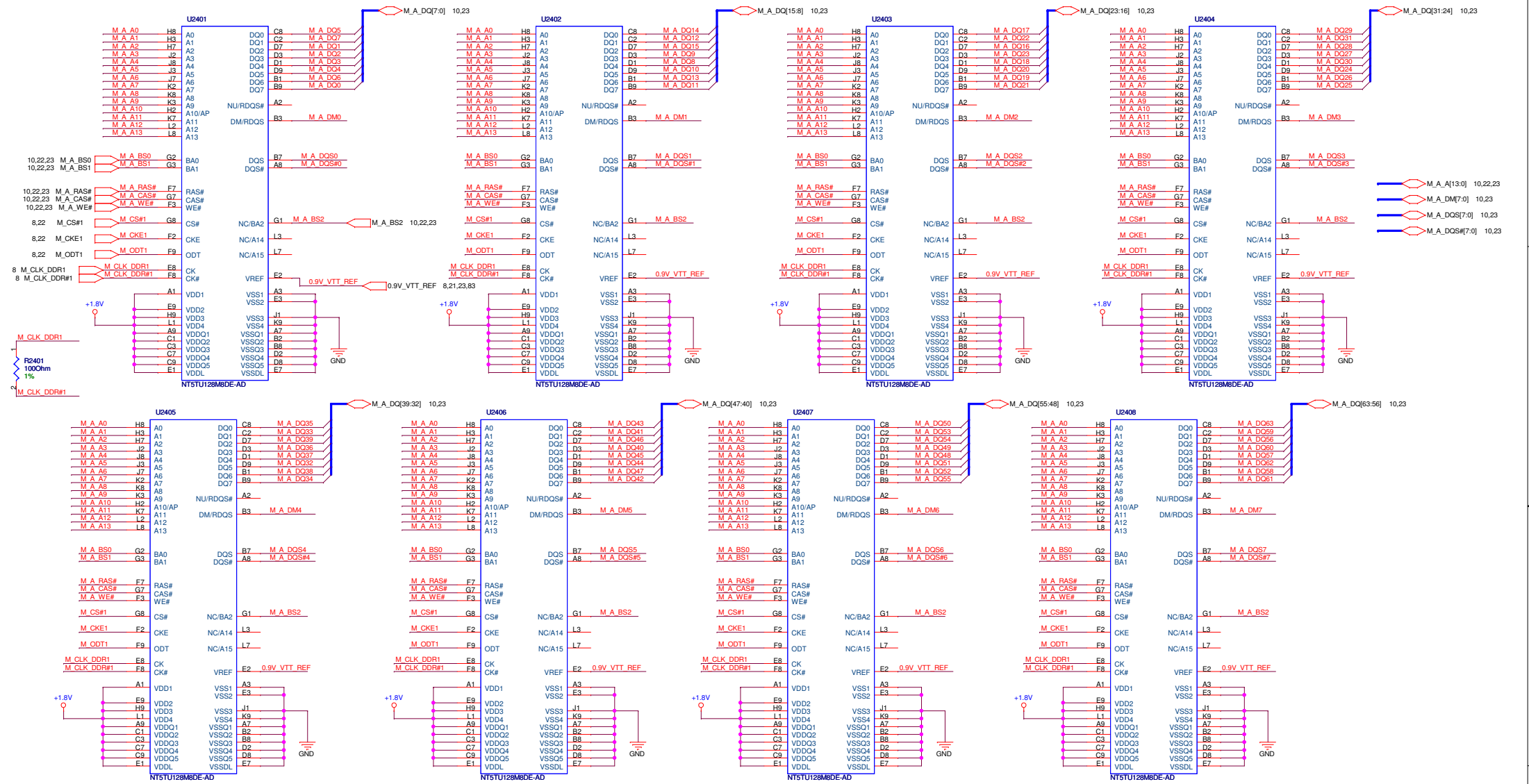
Date: **Monday, March 09, 2009** Sheet **21** of **96**



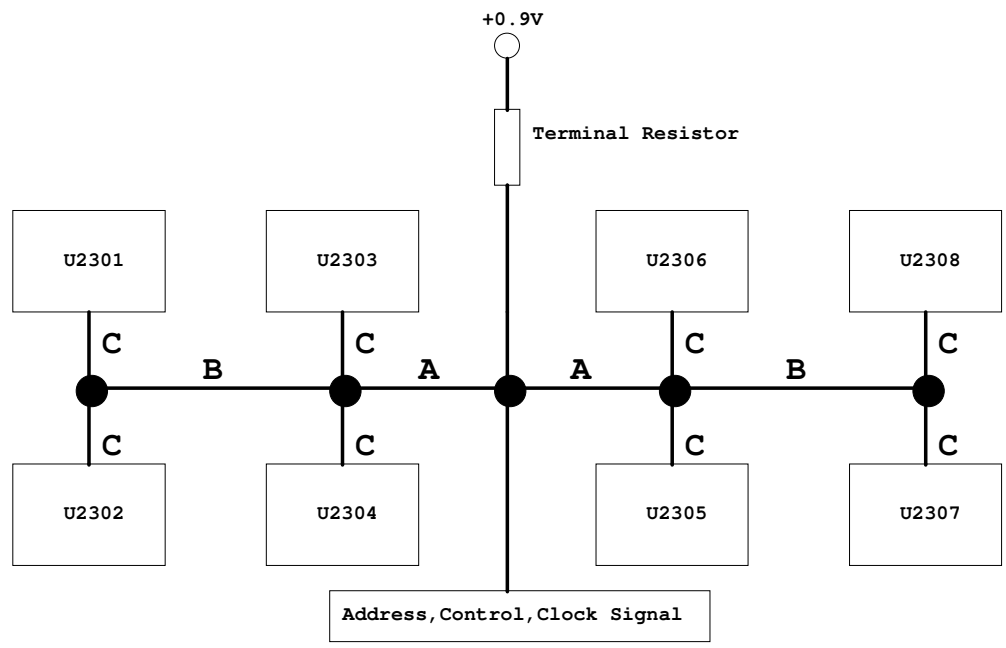
<Variant Name>

<b>ASUS</b>		<b>Title : DDR2 TERMINATION</b>	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009	Sheet	22	of 96









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<Variant Name>

		<b>Title : Schematic page name</b>	
ASUSTek COMPUTER INC		<b>Engineer: Alex&amp;Bruce</b>	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	26 of 96

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<Variant Name>

		<b>Title : Schematic page name</b>	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	27 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTek COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	28 of 96

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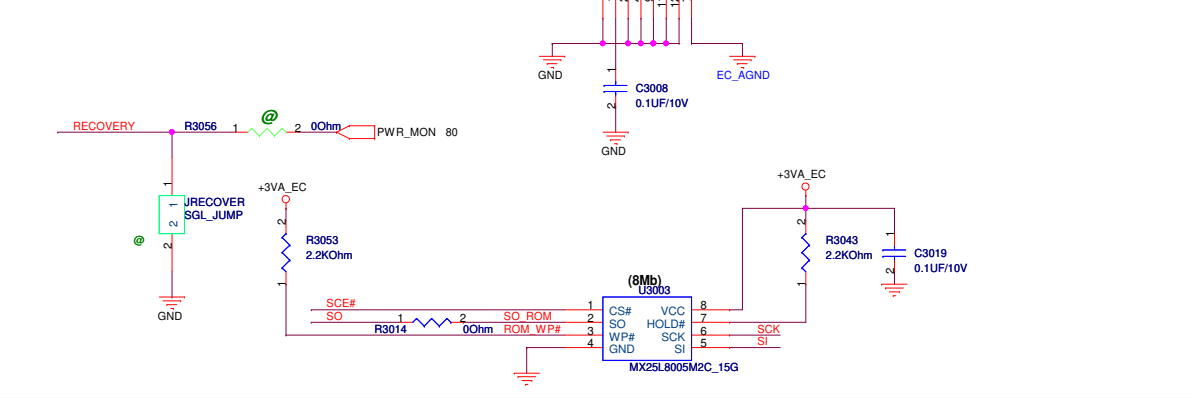
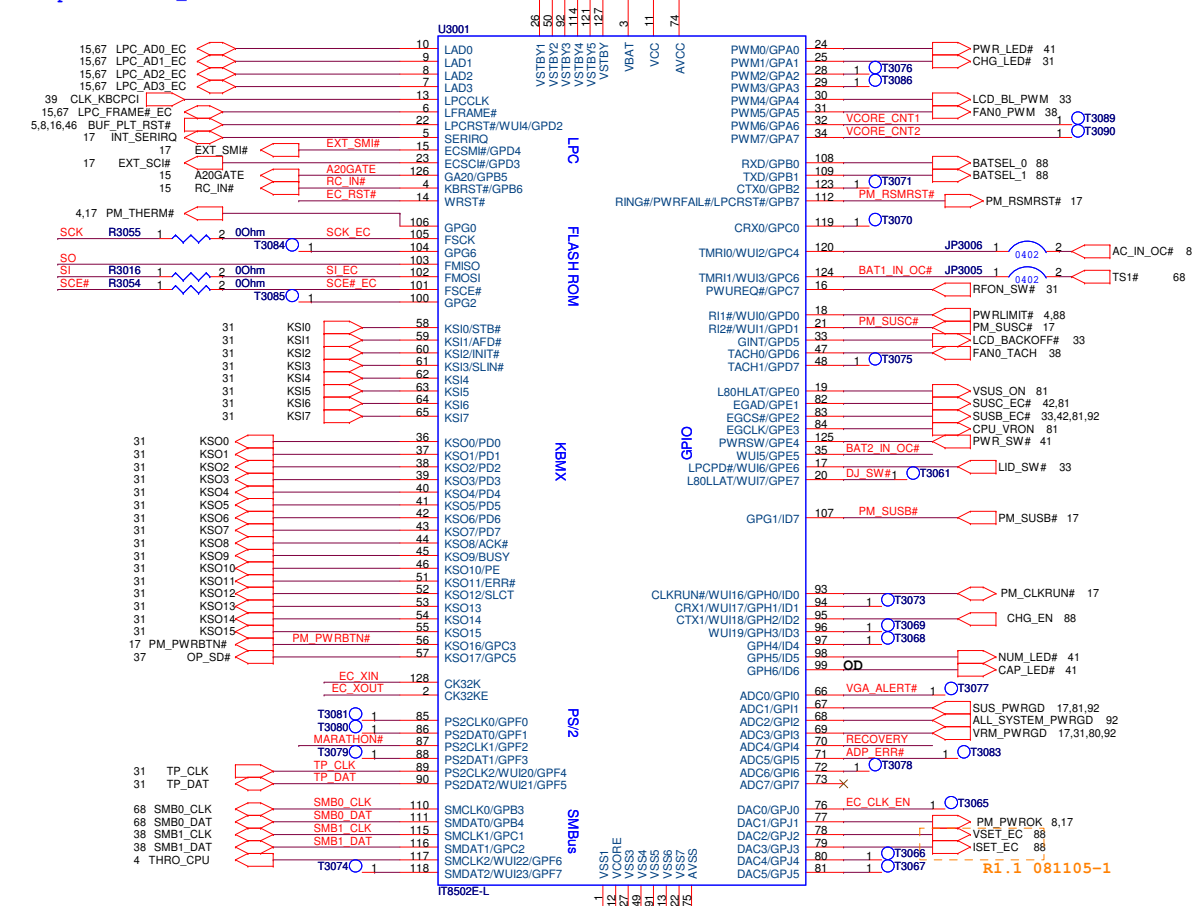
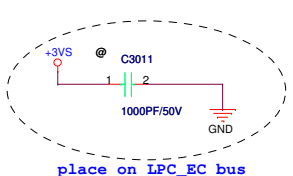
B

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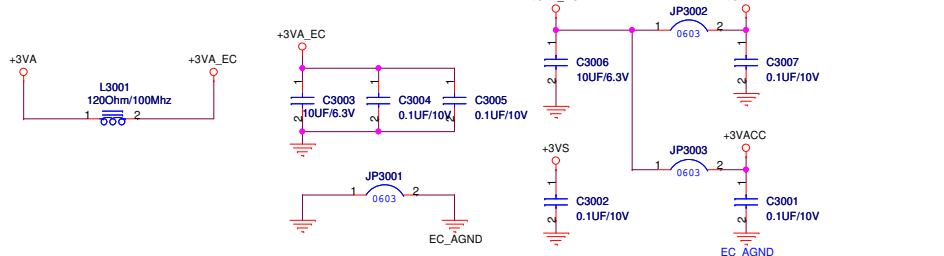
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<Variant Name>

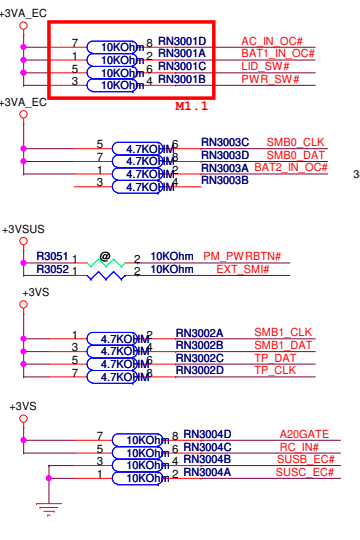
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ASUSTek COMPUTER INC		Engineer: <b>N/A</b>	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
Date: <b>Monday, March 09, 2009</b>		Sheet	29 of 96



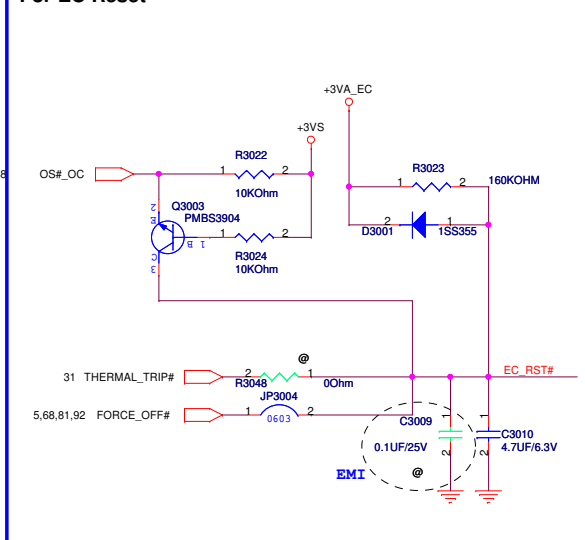
### For IT8702 Power



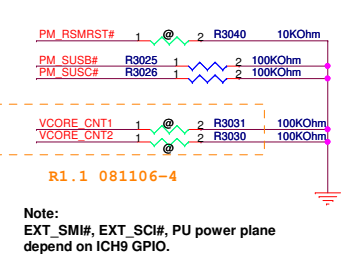
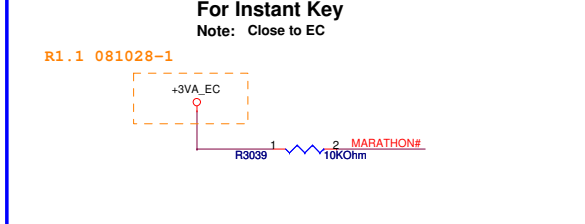
### For PU / PD



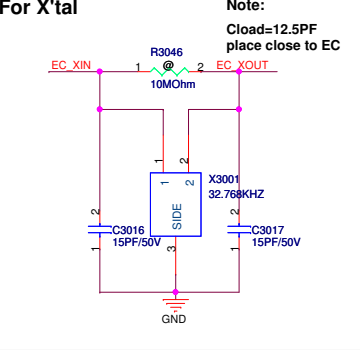
### For EC Reset



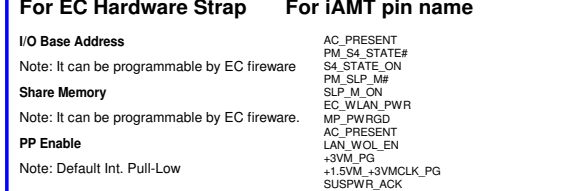
### For Instant Key



### For X'tal



### For EC Hardware Strap

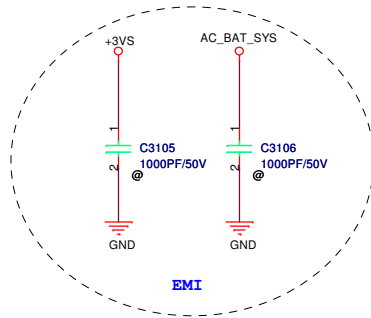
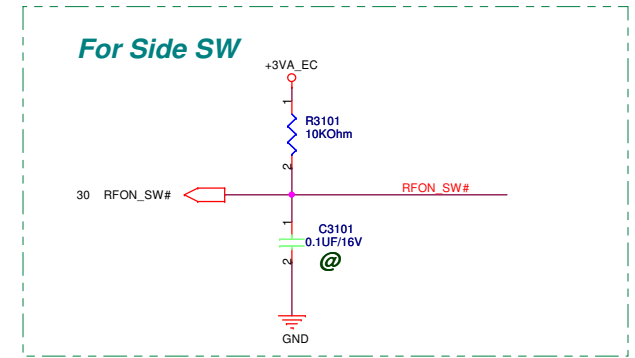
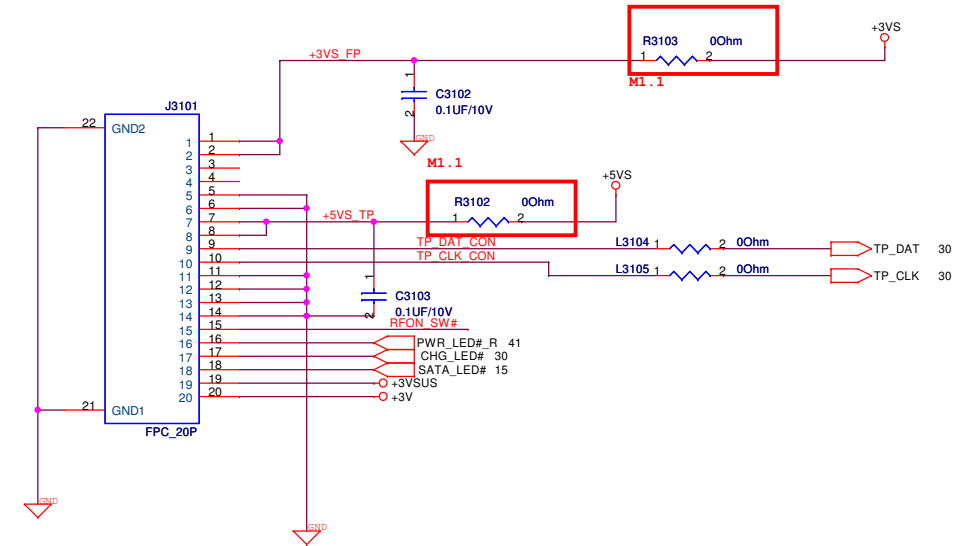


**For iAMT pin name**

- AC\_PRESENT
- PM\_S4\_STATE#
- S4\_STATE\_ON
- PM\_SLP\_M#
- SLP\_M\_ON
- EC\_WLAN\_PWR
- MP\_PWRGD
- AC\_PRESENT
- LAN\_WOL\_EN
- +3VM\_PG
- +1.5VM\_+3VMCLK\_PG
- SUSPWR\_ACK

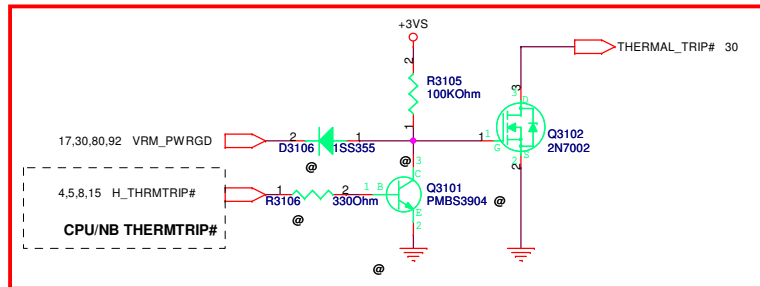
ASUS® Title : EC_IT8512E-L (1/2)	
ASUSTeK COMPUTER INC. NBI Engineer: Wendell Lo	
Size	Project Name
Custom	K40LJ/K50LJ
Date: Monday, March 09, 2009	Sheet 30 of 96

# TouchPad & FingerPrint

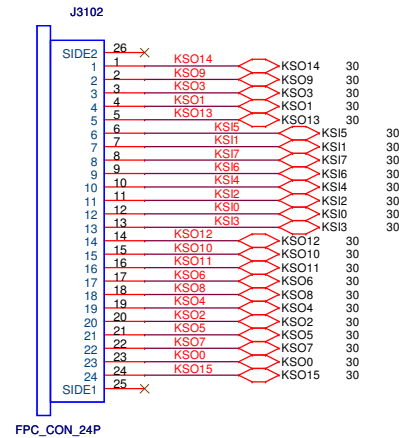


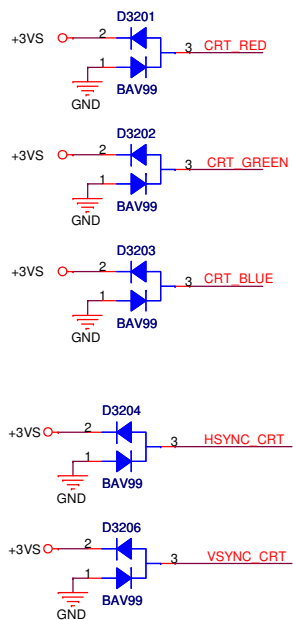
## For Thermal Control Method

Remove redundant components

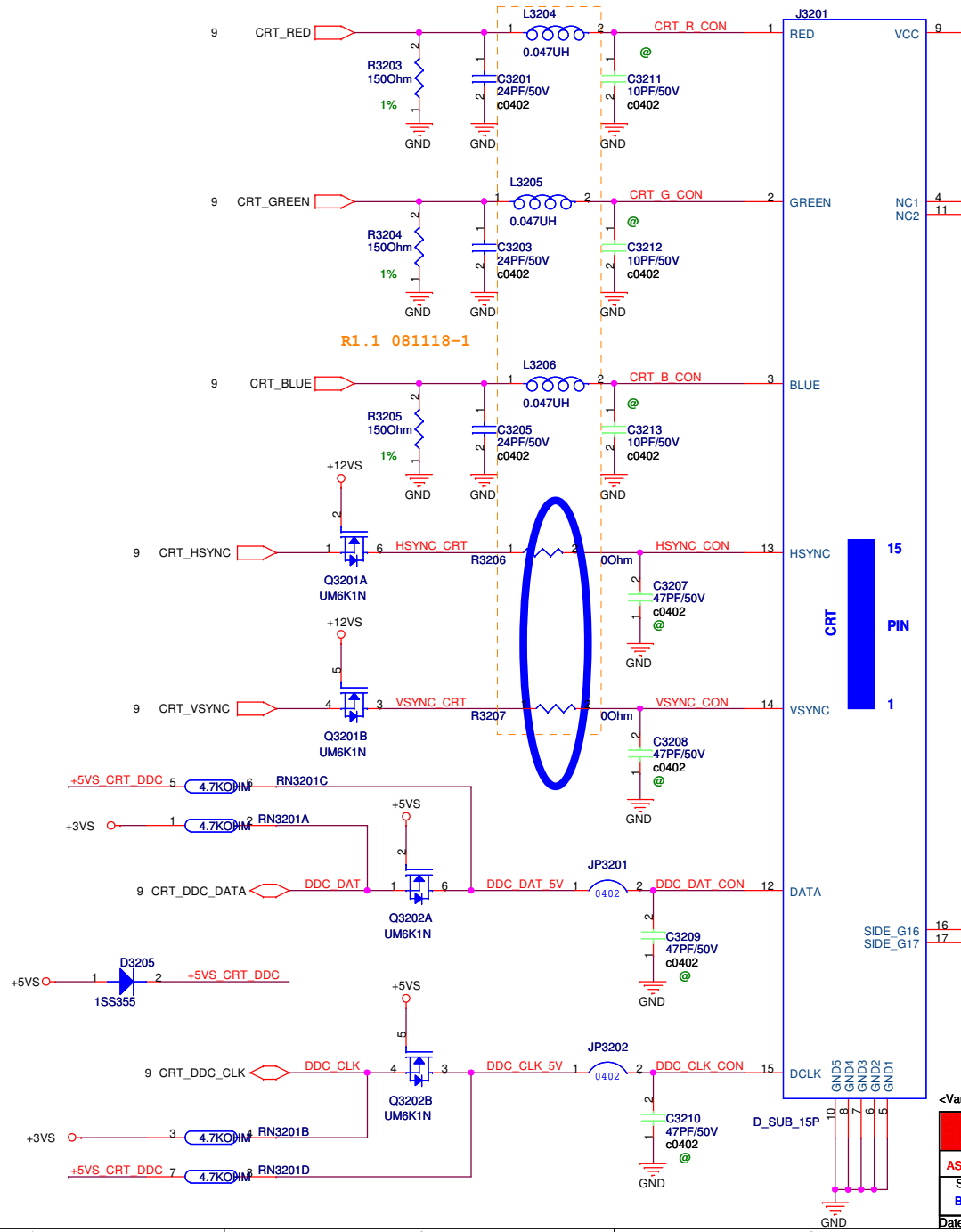


## Keyboard Connector





PLACE ESD Diodes near VGA port

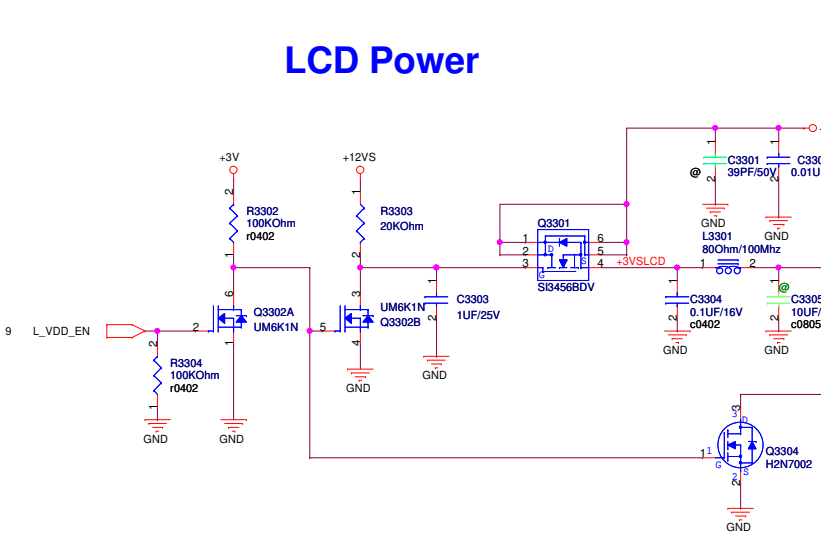


<Variant Name>

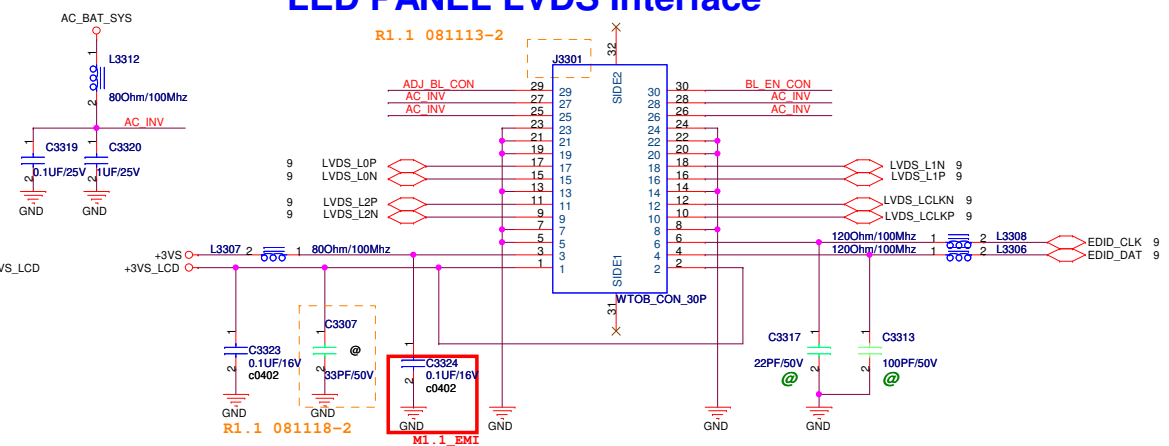
		<b>Title : CRT</b>
ASUSTeK COMPUTER INC		Engineer: N/A
Size B	Project Name <b>K401J/K501J</b>	Rev 1.1
Date: Monday, March 09, 2009	Sheet 32	of 96



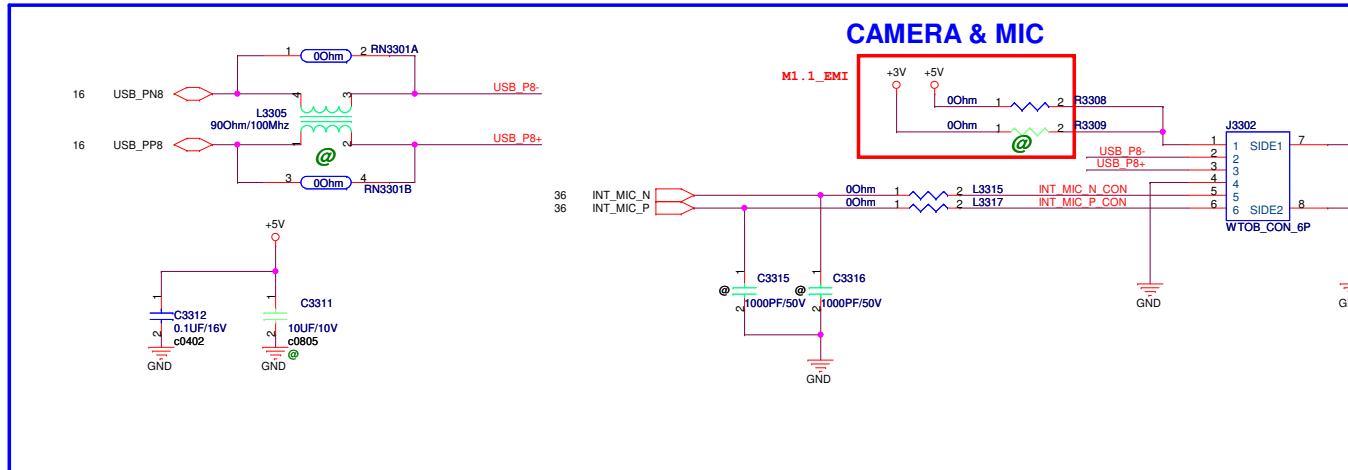
# LCD Power



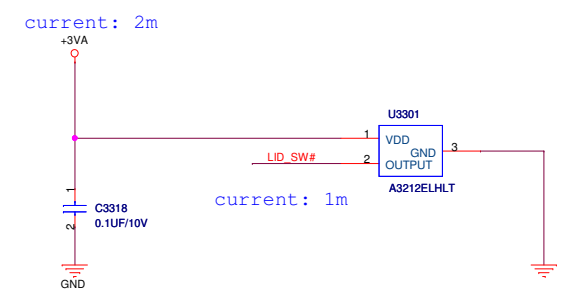
# LED PANEL LVDS Interface



# CAMERA & MIC



# Hall effect switch



R1.1 081029-1

R1.1 081113-2

R1.1 081118-2

M1.1\_EMI

<Variant Name>

<b>ASUS</b>		<b>Title : LVDS &amp; INVERTER</b>	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	<b>K40LJ/K50LJ</b>		1.1
Date: Monday, March 09, 2009	Sheet	33	of 96

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*For Bluetooth*

<Variant Name>

		<b>Title : BT</b>	
ASUSTeK COMPUTER INC		<b>Engineer: N/A</b>	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
Date: Monday, March 09, 2009		Sheet	34 of 96

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<Variant Name> 		<b>Title :</b> N/A
ASUSTek COMPUTER INC		<b>Engineer:</b> N/A
Size A	Project Name <b>K40IJ/K50IJ</b>	Rev 1.1
Date: Monday, March 09, 2009		Sheet 35 of 96

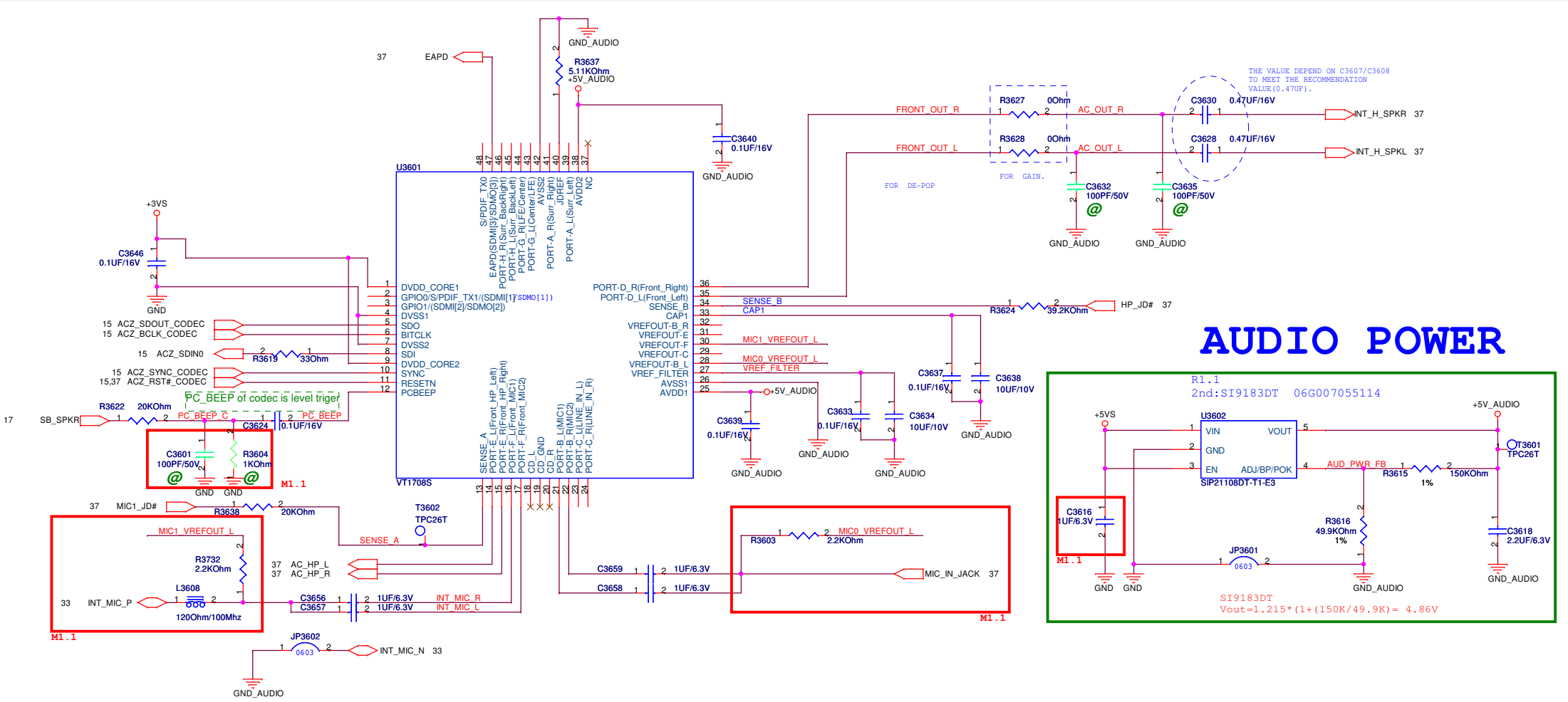
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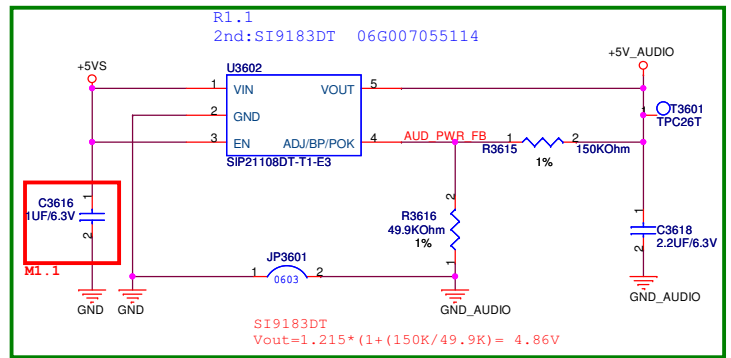
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# AUDIO POWER



THE VALUE DEPEND ON C3607/C3608 TO MEET THE RECOMMENDATION VALUE (0.47UF).

<Variant Name>

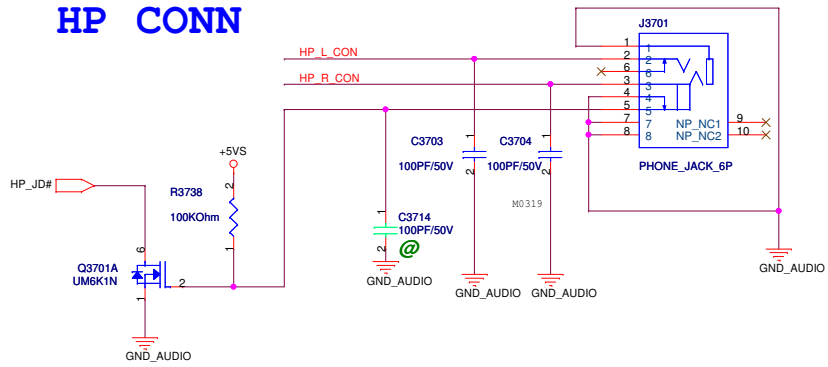
**ASUS** Title : CONEXANT CX20582

ASUSTeK COMPUTER INC Engineer: N/A

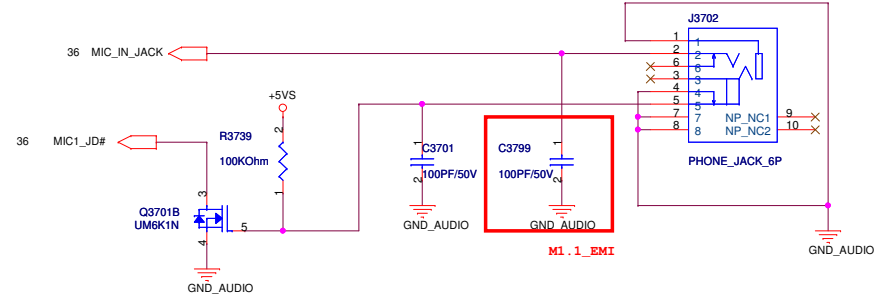
Size	Project Name	Rev
Custom	<b>K401J/K501J</b>	1.1

Date: Monday, March 09, 2009 Sheet 36 of 96

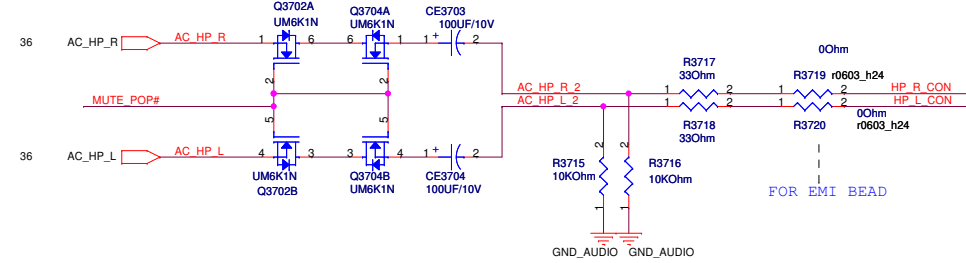
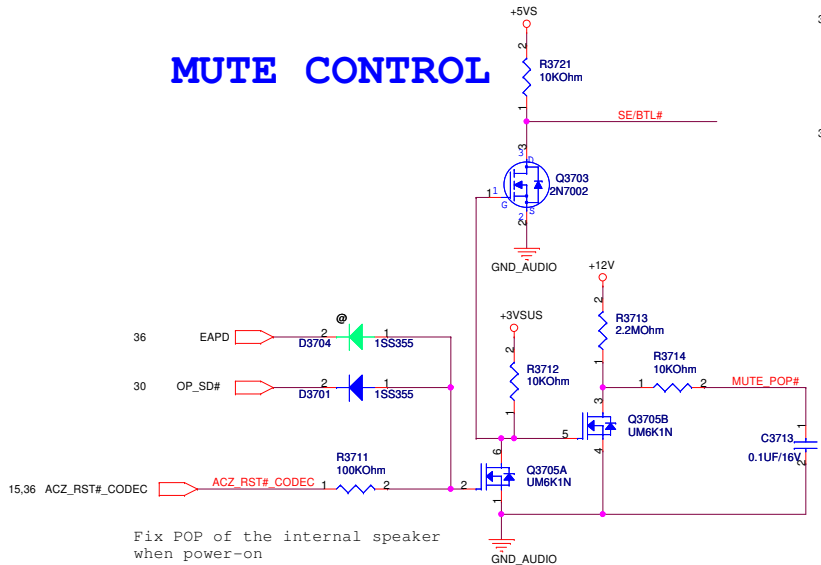
# HP CONN



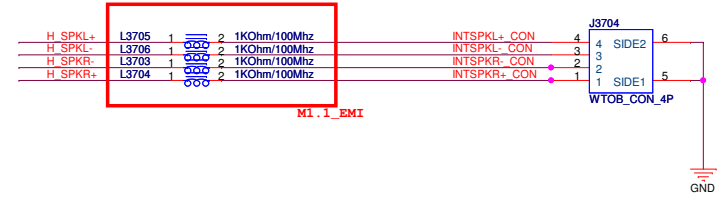
# External MIC CONN



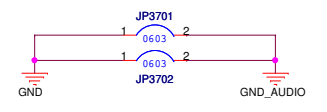
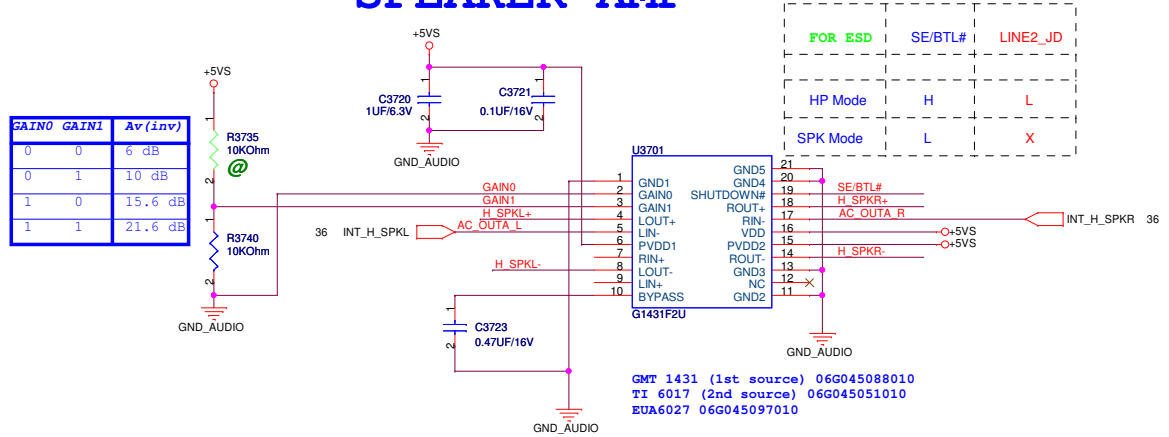
# MUTE CONTROL



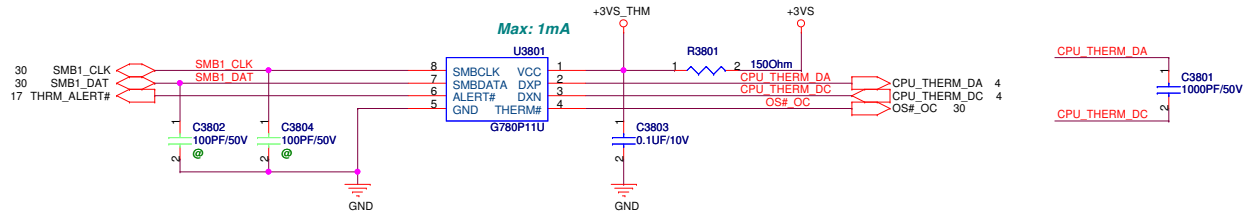
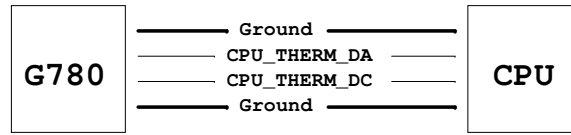
# SPEAKER CONNECTOR (2W)



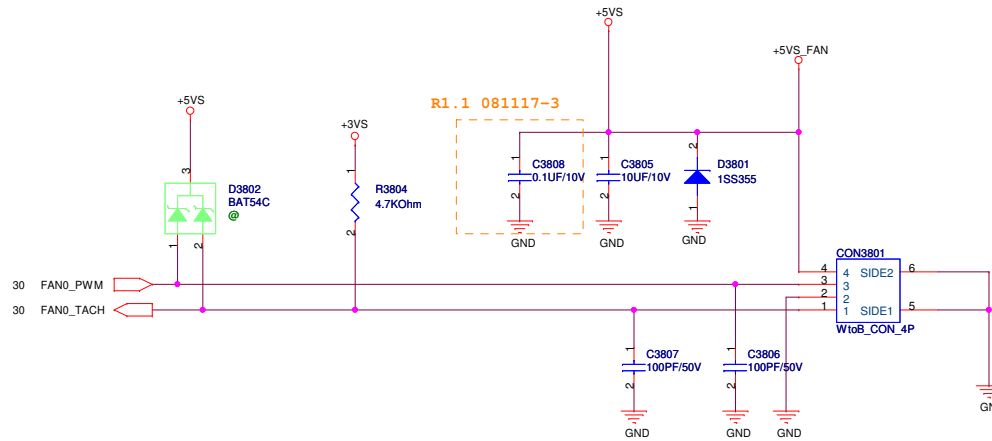
# SPEAKER AMP



# Thermal Sensor

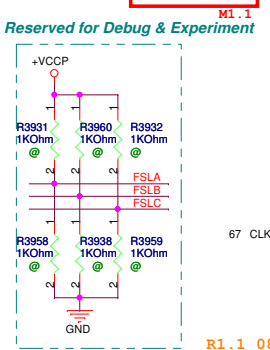
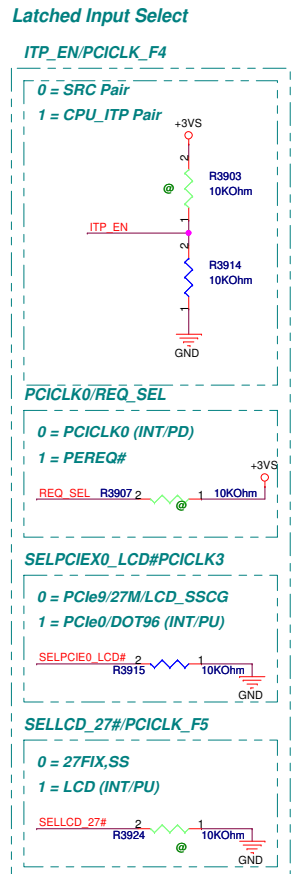
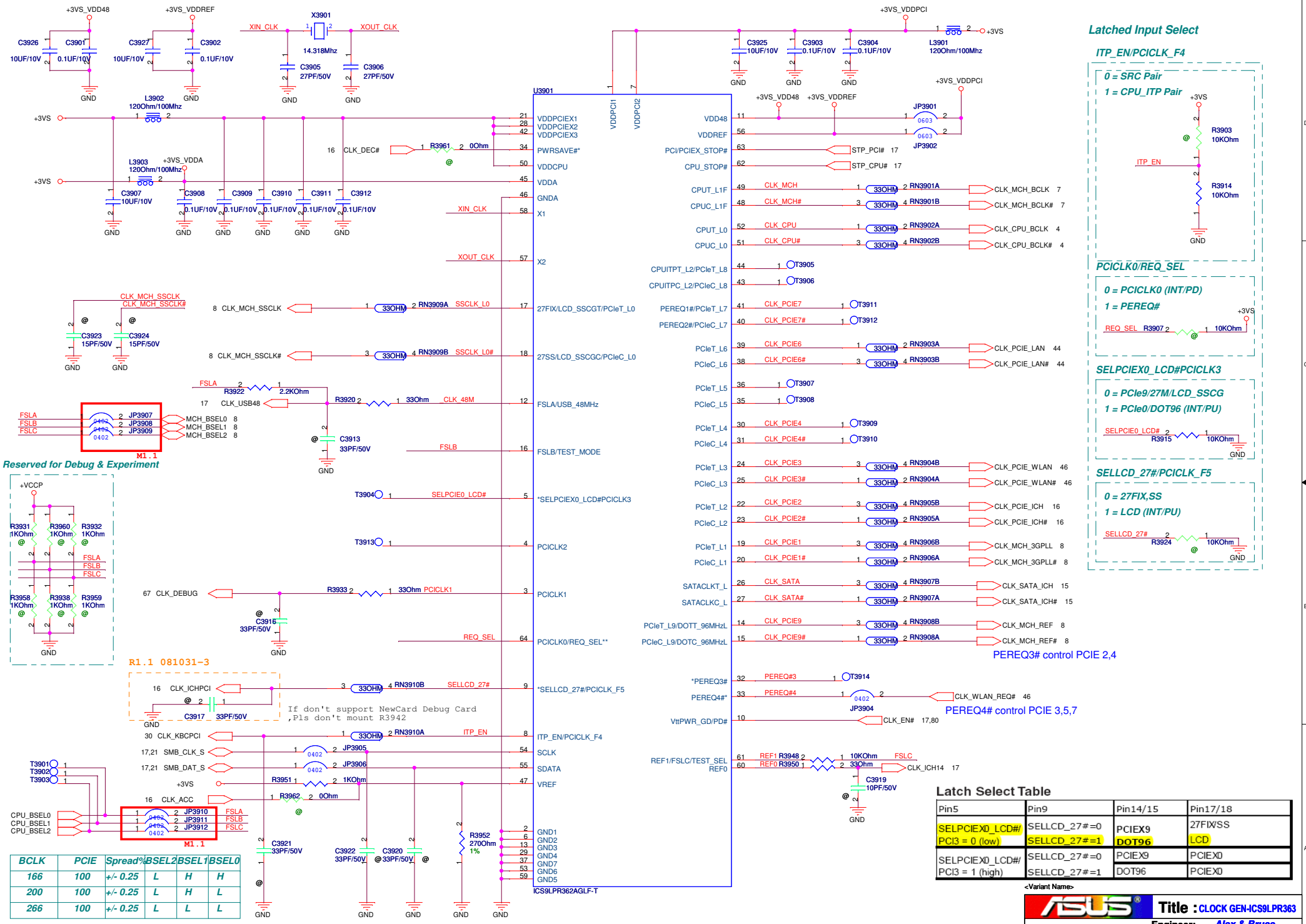


add 2nd source :06G023096010



<Variant Name>

<b>ASUS</b>		<b>Title : THER SENSOR &amp; FAN</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	<b>K40J/K50J</b>	1.1	
Date: Monday, March 09, 2009		Sheet	38 of 96



BCLK	PCIE	Spread%	BSEL2	BSEL1	BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L
266	100	+/- 0.25	L	L	L

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD# PCI3 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	27FIX/SS LCD
SELPCIE0_LCD# PCI3 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	PCIE0 PCIE0

**ASUS** Title: **CLOCK GEN-ICS9LPR363**  
**ASUSTek COMPUTER INC. NB1** Engineer: **Alex & Bruce**  
 Size: Custom Project Name: **K40IJ/K50IJ** Rev: 1.1  
 Date: Monday, March 09, 2009 Sheet: 39 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date:	Monday, March 09, 2009	Sheet	40 of 96

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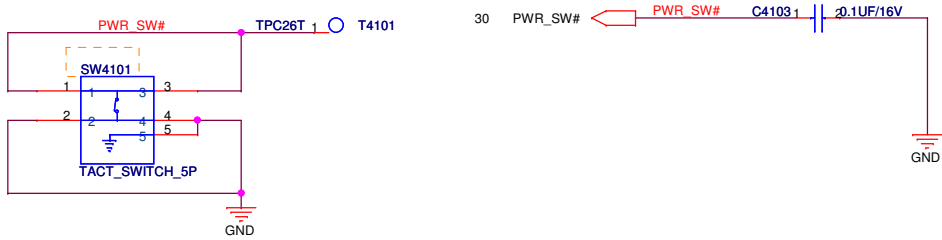
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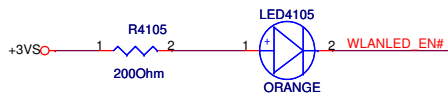


# SWITCH BUTTON

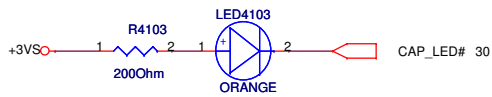


# LED

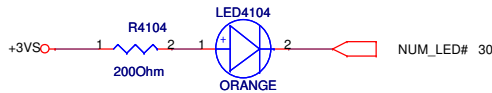
For WireLess LED



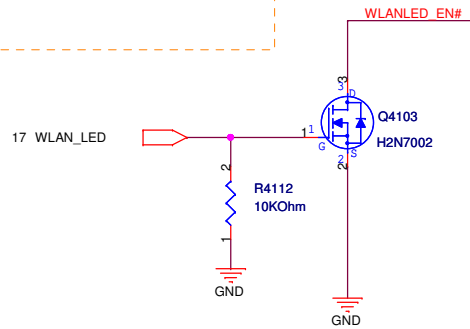
for Cap. Lock



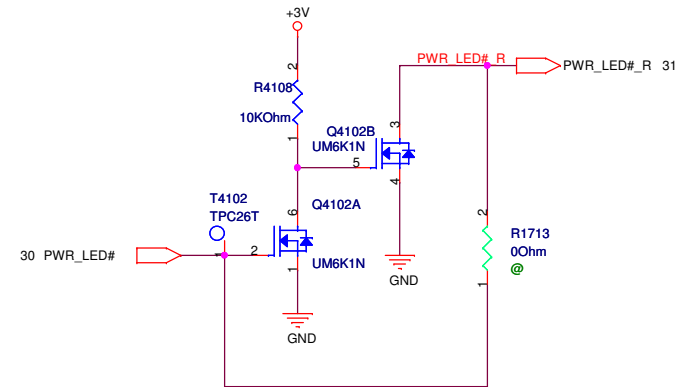
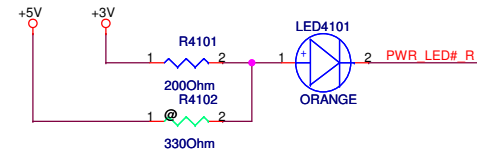
for Num Lock



R1.1 081031-4

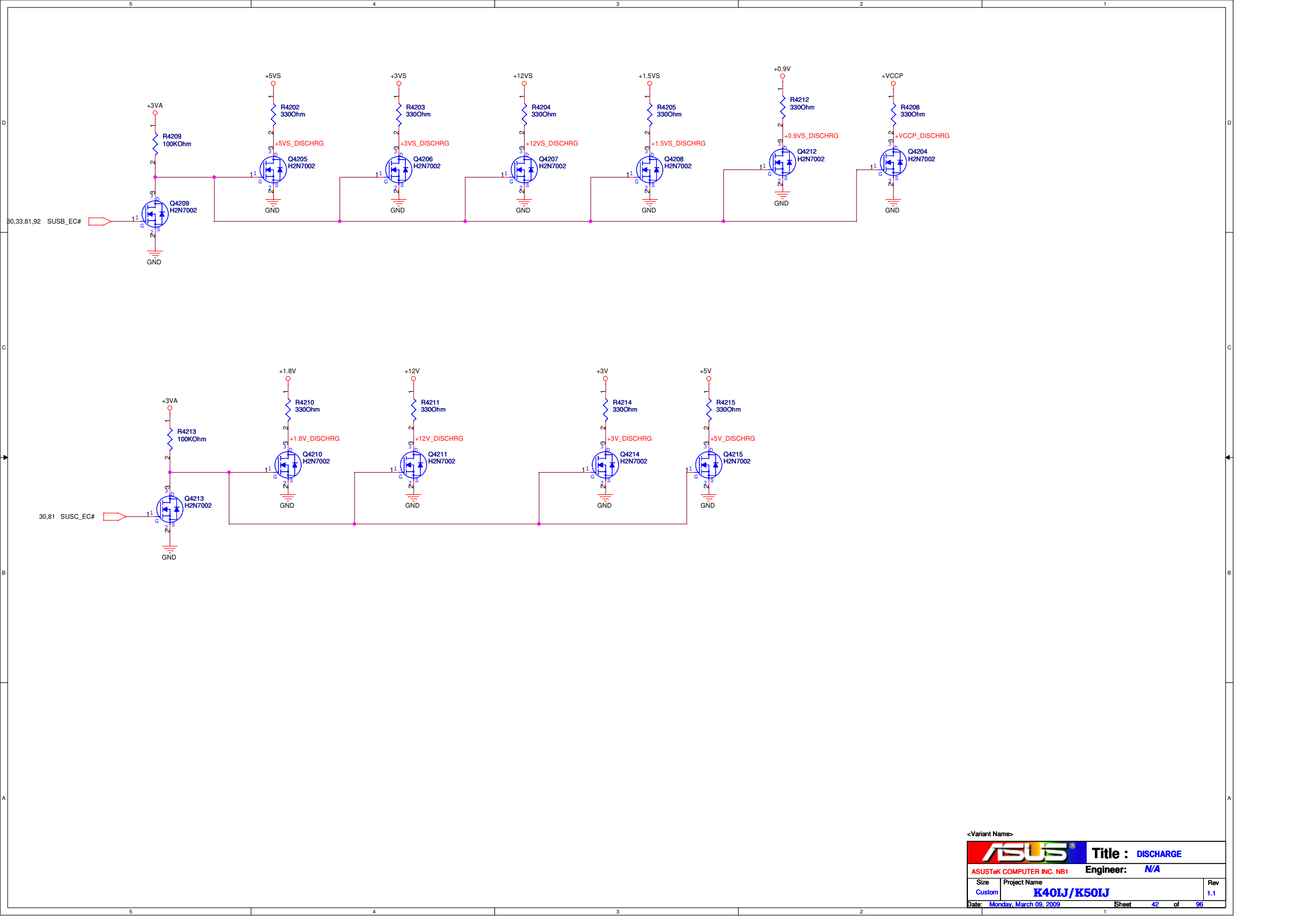


For POWER LED



<Variant Name>

<b>ASUS</b>		<b>Title :Switch Button &amp; LED</b>	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
B	<b>K401J/K501J</b>	1.1	
Date: Monday, March 09, 2009		Sheet	41 of 96



<Variant Name>

		<b>Title : DISCHARGE</b>	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	<b>K40J/K50J</b>		1.1
Date: Monday, March 09, 2009	Sheet	42	of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date:	Monday, March 09, 2009	Sheet	43 of 96

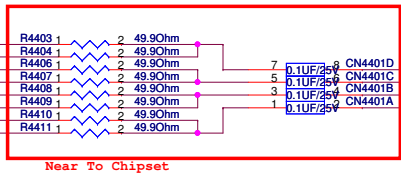
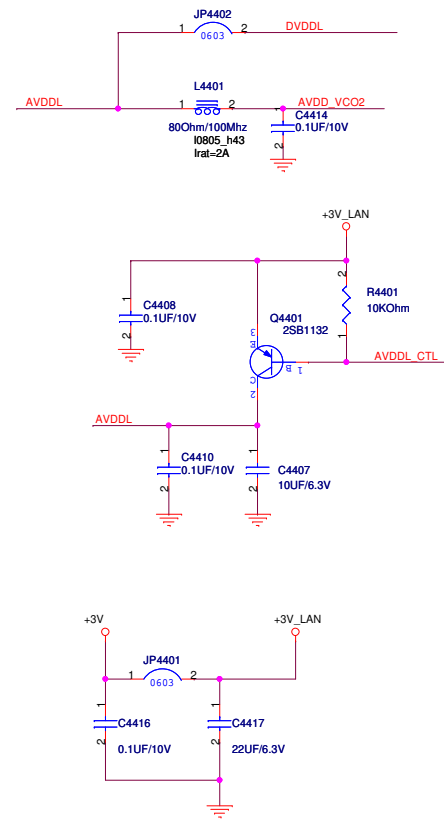
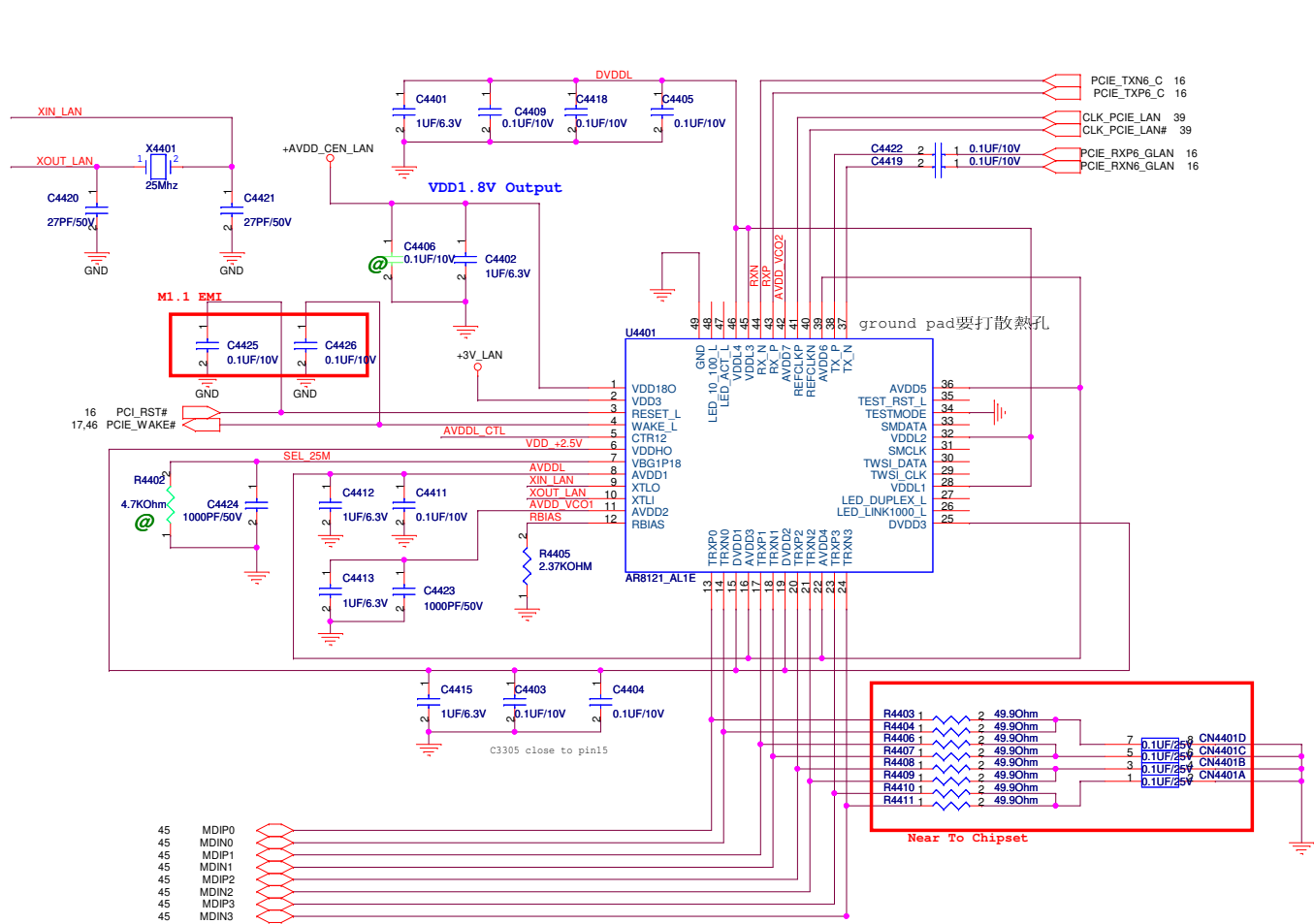
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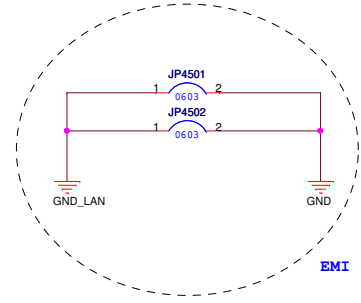
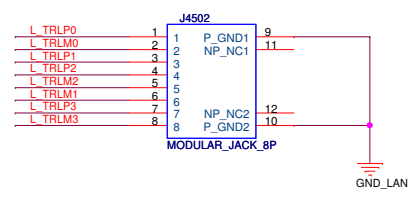
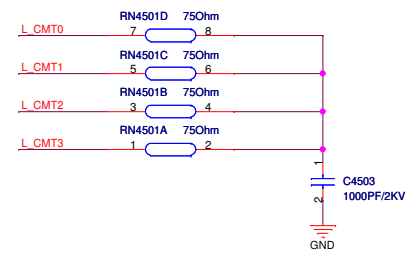
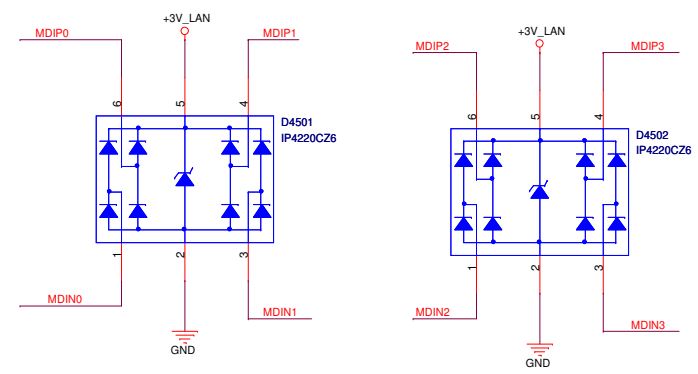
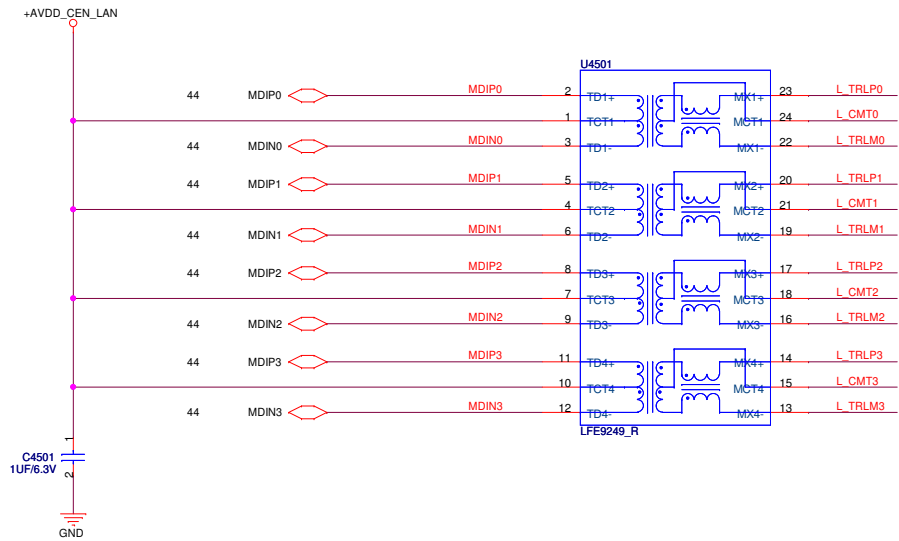
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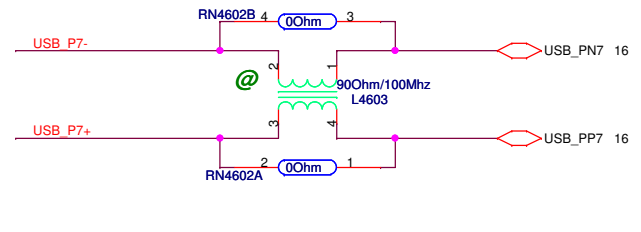
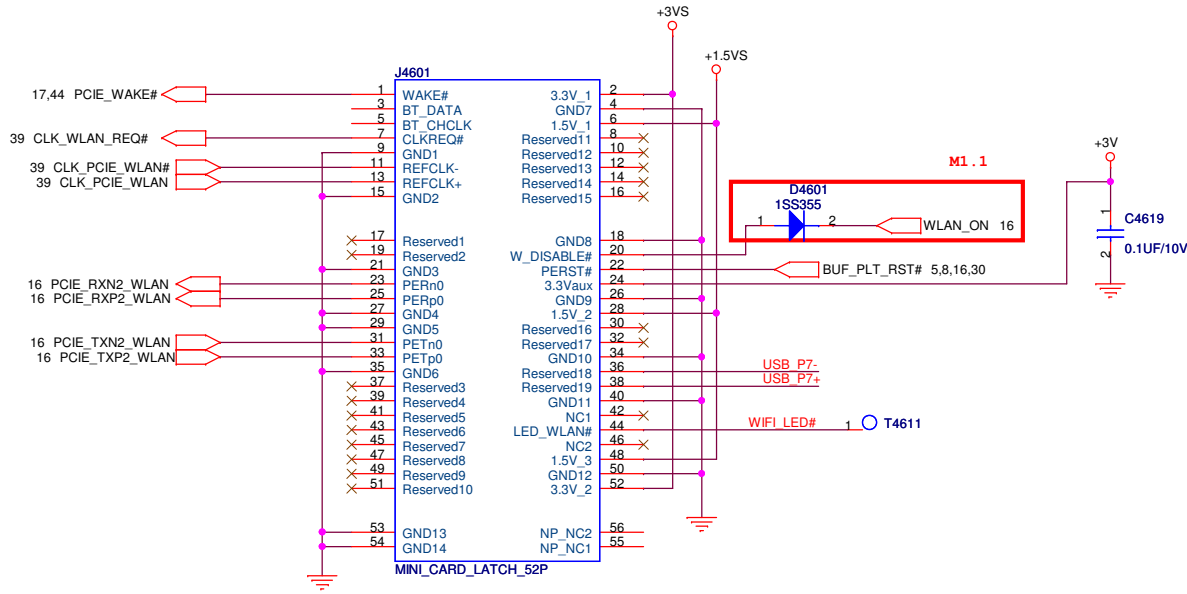
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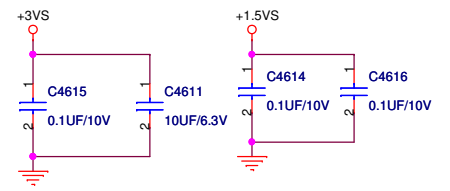


# LAN CONN.





WLAN H=7.5mm



<Variant Name>

<b>ASUS</b>		<b>Title :Mini card_WLAN+3G</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
Date: Monday, March 09, 2009		Sheet	46 of 96

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<Variant Name>



Title : N/A

ASUSTeK COMPUTER INC. NB1 Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009 Sheet 47 of 96

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<Variant Name>

		<b>Title :Schematic page name</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer: N/A</b>	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
Date: Monday, March 09, 2009	Sheet	48	of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	49 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	50 of 96

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<Variant Name>

		<b>Title : N/A</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer: N/A</b>	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
Date: Monday, March 09, 2009		Sheet	51 of 96

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<Variant Name>

		<b>Title :</b> N/A	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
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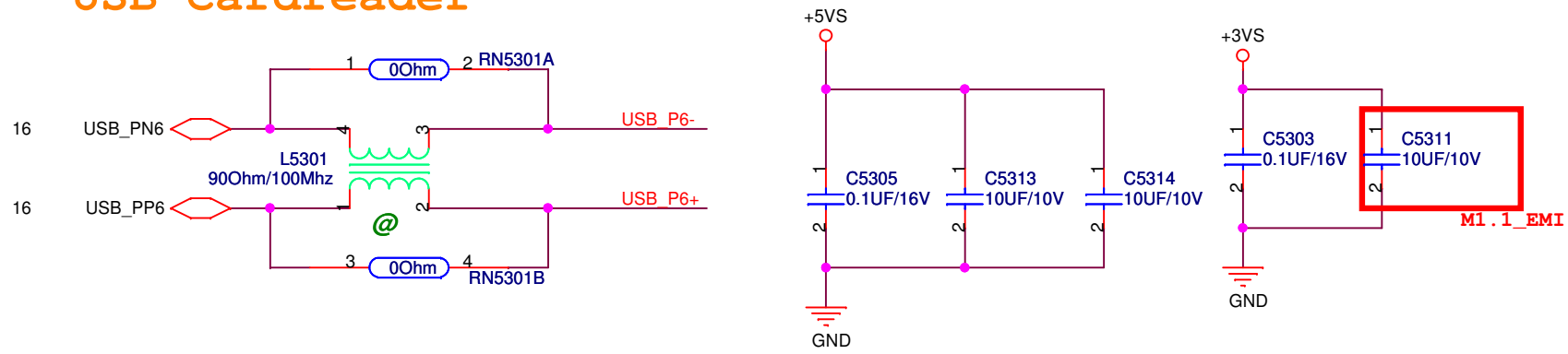
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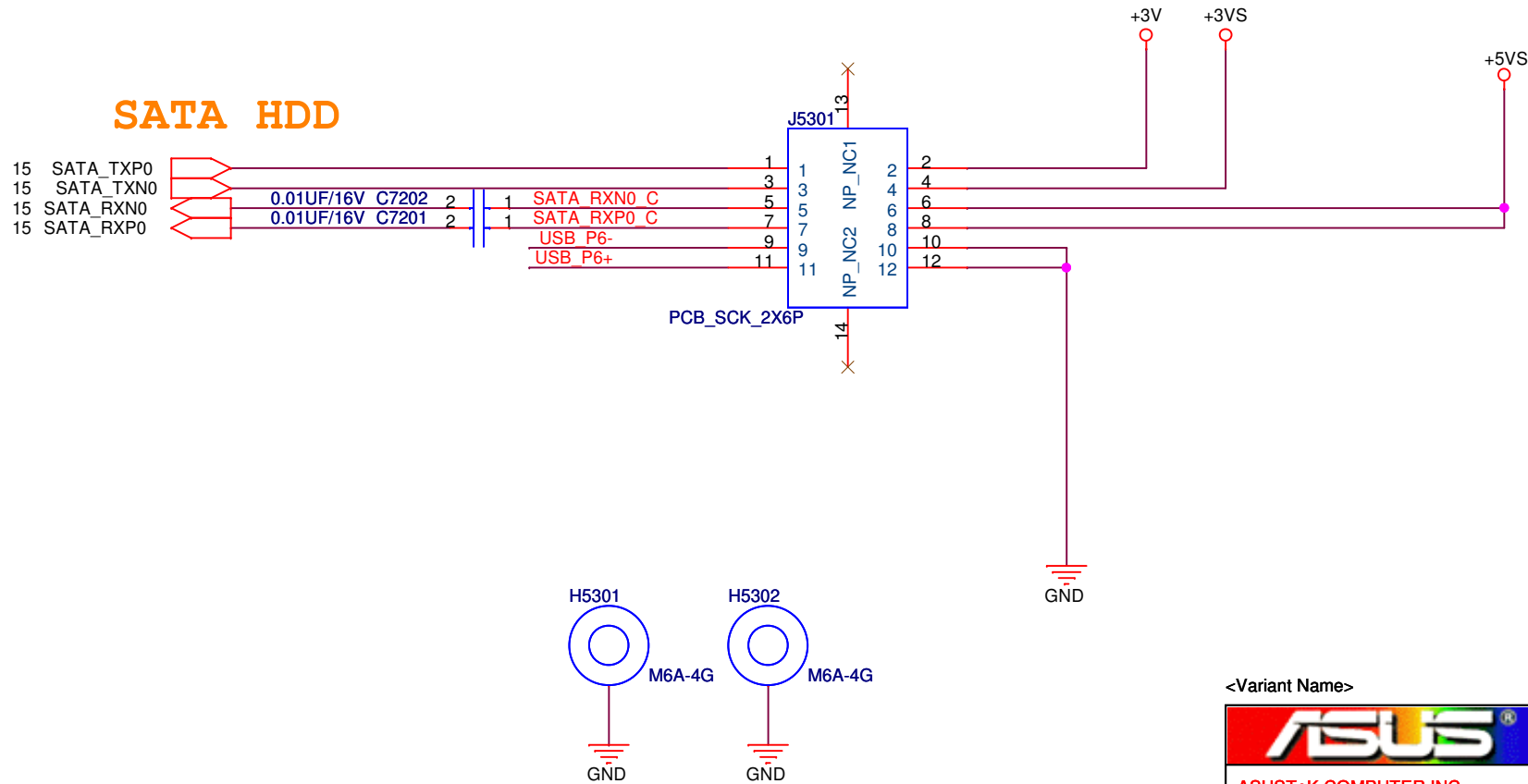
2

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# USB Cardreader



# SATA HDD



<Variant Name>

		<b>Title :SATA_HDD &amp; Cardreader</b>	
ASUSTeK COMPUTER INC		Engineer: <b>N/A</b>	
Size Custom	Project Name <b>K40IJ/K50IJ</b>		Rev 1.1
Date: <b>Monday, March 09, 2009</b>		Sheet <b>53</b> of <b>96</b>	

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<Variant Name>

		<b>Title :</b> NEWCARD
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A
Size	Project Name	Rev
B	<b>K40IJ/K50IJ</b>	1.1
Date: Monday, March 09, 2009		Sheet 54 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date:	Monday, March 09, 2009	Sheet	55 of 96

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<Variant Name>

		<b>Title : HDA level shifter</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>N/A</i>	
Size Custom	Project Name <b>K40LJ/K50LJ</b>		Rev 1.1
Date: <i>Monday, March 09, 2009</i>		Sheet <i>56</i> of <i>96</i>	

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# HDMI WtoB Connector

# HDCP ROM

<Variant Name>

		<b>Title :</b> iHDMI
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A
<b>Size</b> B	<b>Project Name</b>	<b>Rev</b> 1.1
<b>Date:</b> Monday, March 09, 2009		<b>Sheet</b> 57 <b>of</b> 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
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<Variant Name>



Title : Schematic page name

ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date:	Monday, March 09, 2009	Sheet	61 of 96

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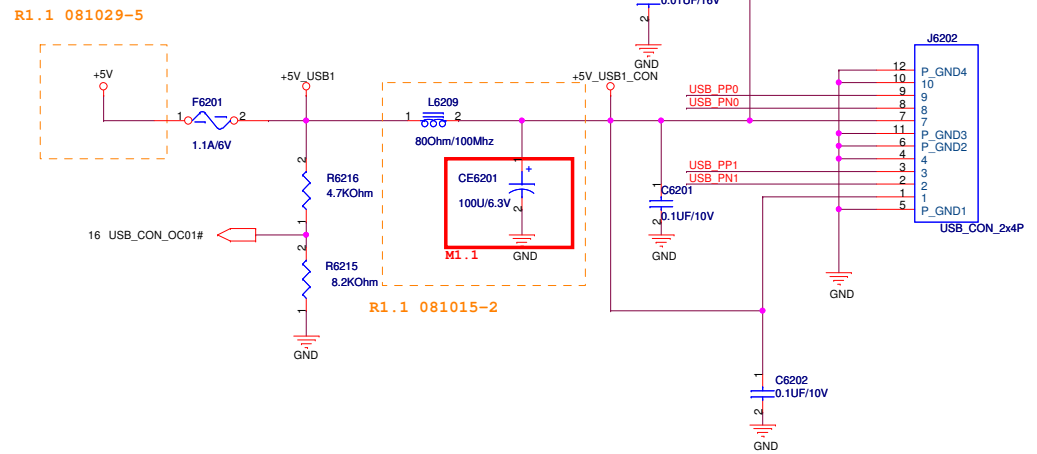
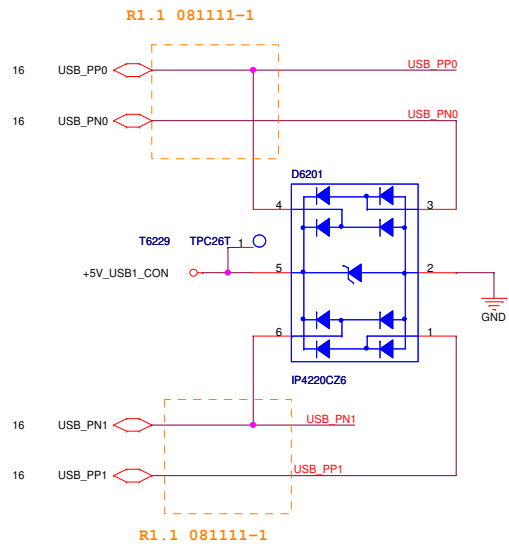
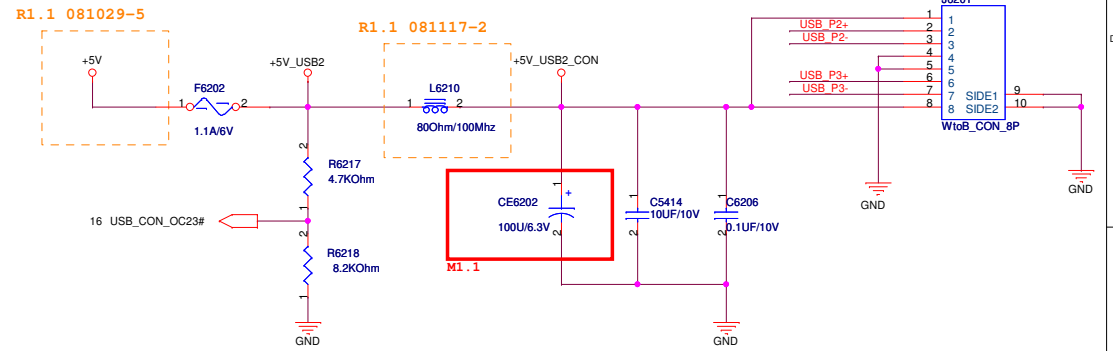
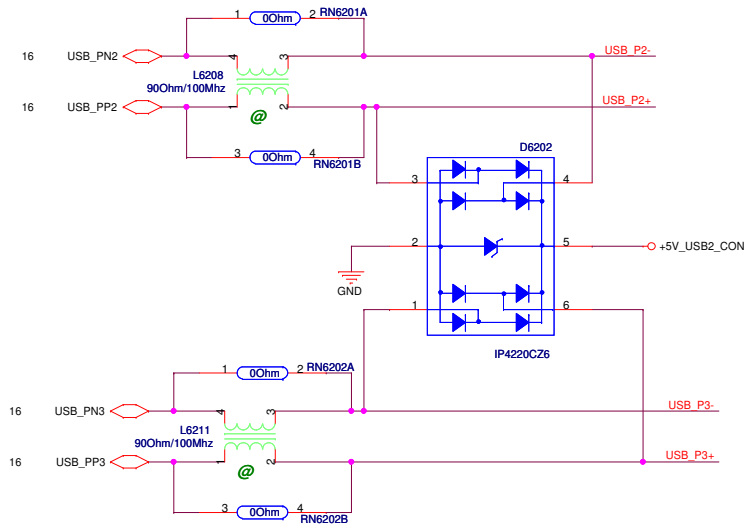
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# USB IO Board



<Variant Name>

<b>ASUS</b>		<b>Title : USB CONN</b>	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	<b>K40J/K50J</b>	1.1	
Date:	Monday, March 09, 2009	Sheet	62 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
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<Variant Name>



ASUSTeK COMPUTER INC. NB1 Engineer: N/A

Size	Project Name	Rev
Custom	<b>K40IJ/K50IJ</b>	1.1

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<Variant Name>

		<b>Title : SPI ROM</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
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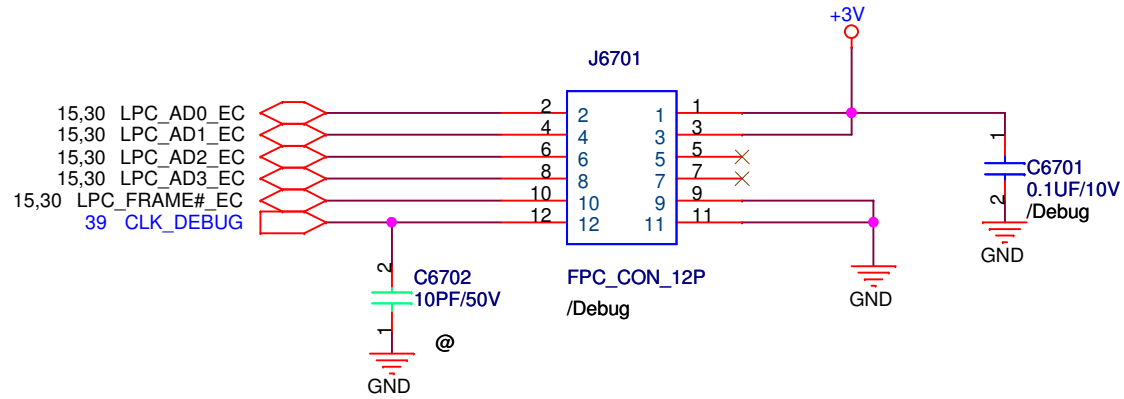
A

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<Variant Name>

		<b>Title : LED</b>	
ASUSTeK COMPUTER INC		<b>Engineer: N/A</b>	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	66 of 96

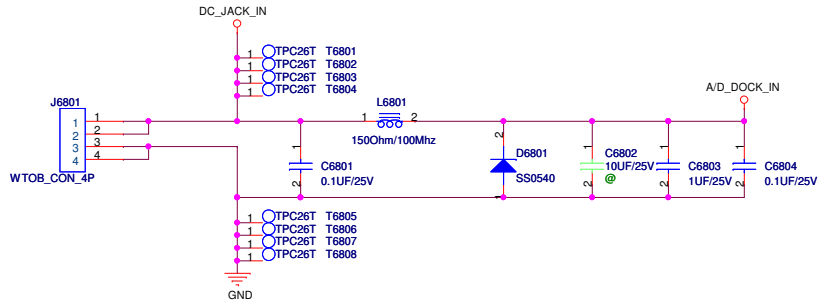
# LPC DEBUG PORT



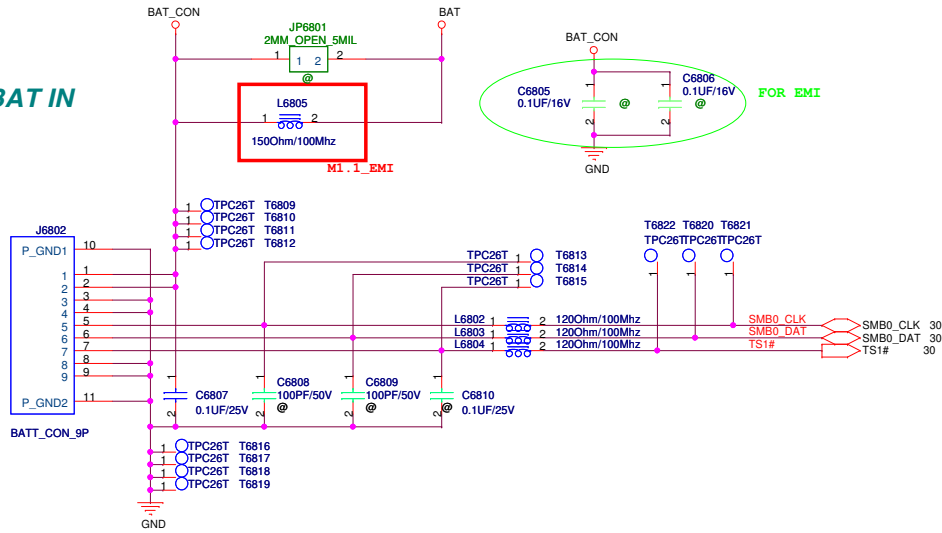
<Variant Name>

<b>ASUS</b>		<b>Title : DEBUG CONN</b>
ASUSTeK COMPUTER INC		Engineer: N/A
Size A	Project Name <b>K40IJ/K50IJ</b>	Rev 1.1
Date: Monday, March 09, 2009		Sheet 67 of 96

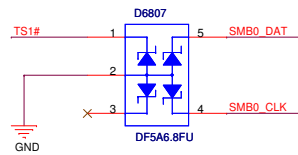
# DC IN



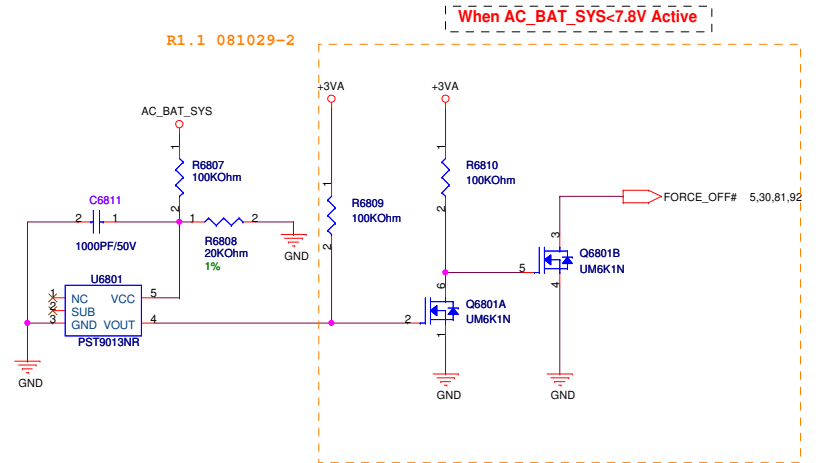
# BAT IN



**Note:** When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.



# Without Battery & Pull out Adapter



<Variant Name>

<b>ASUS</b>		<b>Title : DC &amp; BAT IN</b>	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	<b>K40J/K50J</b>	1.1	
Date: Monday, March 09, 2009	Sheet	68	of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	69 of 96

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<Variant Name>

		<b>Title : Debug CONN.</b>	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	70 of 96

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date:	Monday, March 09, 2009	Sheet	71 of 96

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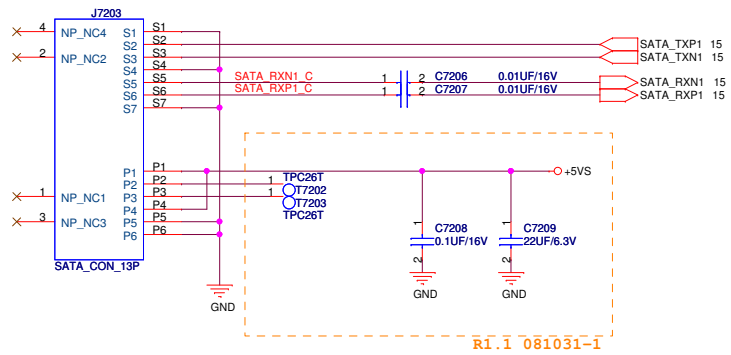
4

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# ODD



<Variant Name>

<b>ASUS</b>		<b>Title : SATA-ODD</b>
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1
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<Variant Name>

		<b>Title :</b> N/A	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> N/A	
Size	Project Name		Rev
Custom	<b>K40IJ/K50IJ</b>		1.1
Date: Monday, March 09, 2009		Sheet	73 of 96

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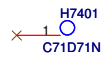
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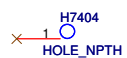
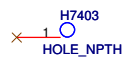
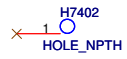
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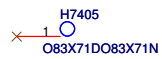
Hole-A



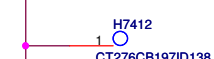
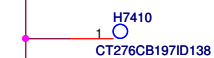
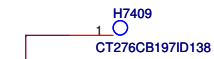
Hole-B



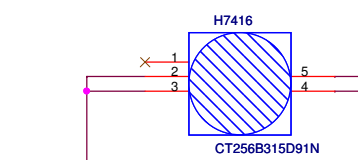
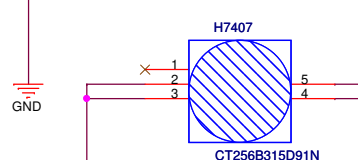
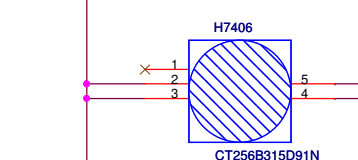
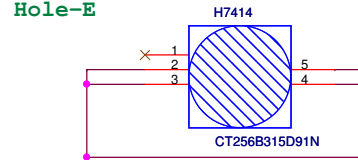
Hole-C



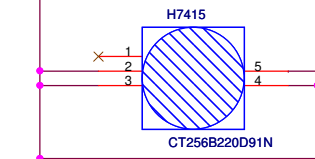
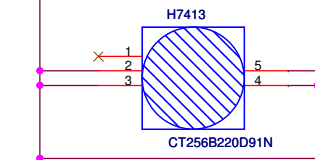
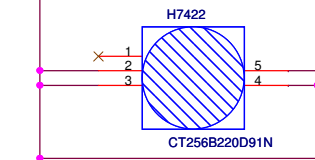
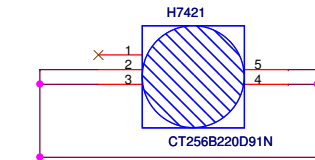
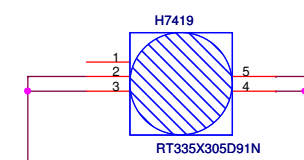
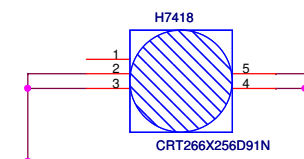
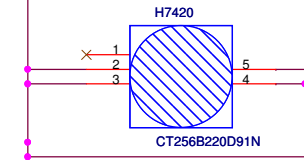
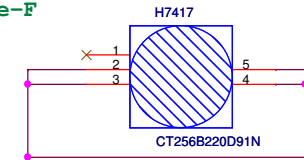
Hole-D



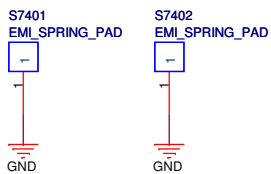
Hole-E



Hole-F



Spring



<Variant Name>

		<b>Title : Hole</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Leon Guo</b>	
Size	Project Name		Rev
B	<b>K40IJ/K50IJ</b>		1.1
Date: <b>Monday, March 09, 2009</b>		Sheet	74 of 96

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<Variant Name>

		<b>Title :</b> N/A	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
A	<b>K40IJ/K50IJ</b>	1.1	
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<Variant Name>

	<b>Title :EXPRESS GATE</b>
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ASUSTeK COMPUTER INC	<b>Engineer: N/A</b>
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Size Custom	Project Name <b>K40IJ/K50IJ</b>	Rev 1.1
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R1.1 Modify List 5

P04\_Q0402,R0401 No mount

P36\_INT\_MIC Change

P37\_J2704 speaker\_H\_SPK1+/H\_SPK1-/H\_SPKR+/H\_SPKR- Signal modify,Del R3732

P05\_C80502,C0528,31,32,33,36,43 NO-Stuff

P07\_C0702 NO-Stuff

P08\_R0813 NO-Stuff,R0815/R0816 10K OHM change to 0 OHM(E/R Check if ok change to J8110 to J8113)

R0817 100 OHM Change to Short JP

P12\_C1223,C1245 100F/10V(1206) change to 100F/6.3V(0805) for reduce

P24\_Add On-board memory to 2G

P30\_change "BATSEL\_28#" to "BATSEL\_0"

change "BATSEL\_38#" to "BATSEL\_1"

Merge R3020,21,27,29 to array resistor

P36\_C3616 Y5V change to X7R for reduce component count

P37\_C3720 Y5V change to X7R for reduce component count

P39\_Delete RN3901,RN3902

P44\_Change LAN Chip from RTL8111DL to AN8121

P09\_R0910,11,12 change to RN0901 array package

R3002,03,05,28 change package

P18\_Add C1843,C3324,C2203,C4425,C4426 for EMI

Del R3506

Change ReferenceC7213,03,05,11 to C53013,03,05,11

P16\_For EMI CMOS form Port 4 change to Port 8

P62\_C86202 Change package

P11\_C1125,26,30 0.22UF change to 1UF cost down

P3601\_Reserve C3601,R3604 for Vendor request

F31\_L3102,03 change to R3103,02

Add JP1502 del R1511

Del R0918,R0919 add RN0902

P39\_Del R3946 ,add RN3910

P04\_C0401,02,03 add for EMI

P04\_C0402 add for EMI



P05\_Del JP0501

P16\_Add R1602

P33\_Add R3308,R3309

Power List 1/15

change J8112 to J8112

change J8113 to J8113

change J8114 to J8114

change J8115 to J8115

change J8110 to J8110

change J8113 to J8113

change J8114 to J8114

change J8115 to J8115

change J8103 to J8103

change J8106 to J8106

change J8109 to J8109

change J8111 to J8111

change J8105 to J8105

page 82

change JP8203 to J8203

page 83

change JP8303 to J8303

change JP8304 to J8304

page 84

add JP8402

change U8401 to APL5930 from APL5913

page 88

change JP8805 to J8805

1/14

page 80

change Q8001 and Q8003 to 07G005A15011 from 07G005C34010.

change Q8002 and Q8004 to 07G005B71010 from 07G005C33010.

stuff C8003

page 83

change R8304 to 10G212150214030 from 10G212750114010.

1/08

Change all 2MM\_SHORT\_SMI1 to 2MM\_OPEN\_SMI1(s00496)

page 81

change "L7020\_DLL1" to "8206\_DLL1".

page 88

add L8802 between BAT and BAT\_CON

change R8823.2 to GND from SGND\_CHG.

change "BATSEL\_28#" to "BATSEL\_0"

change "BATSEL\_38#" to "BATSEL\_1"

01/07

Delete Empty Page 85,86,87,89,90

Page 80

Change R8010, R8013, R8020, R8035, R8040, R8046 to temp.4759\_ch01 from 10G212000004010

Change C8003, C8017 to Unmount

Delete R8050

Page 81

Change R8116, R8119, R8125, R8110, R8107 to temp.4759\_ch01 from 10G212000004010

Delete R8102, R8118

Change D8103 to 07G004069020 from 07G001007230

Page 82

Change D8201 to 07G004069020 from 07G001007230

Page 83

Change D8301 to 07G004069020 from 07G001007230

Page 84

Delete R8404

Delete Netname 5913\_VCNFL

Page 88

Change D8804 to 07G004069020 from 07G001007230

Page 91

Change R9105, R9108 to 10G252100314030 from 10G212100314030

12/31

page 80

change Q8002, Q8004 to 07G005C35010 from 07G005C33010

change U8001 to 06G008425013 from 06G008692010

change R8026 to 10G212680114010 from 10G212953114010

12/26

page 81

change CE8101, CE8102 to 11G08D21075A from 11G09X222755.

page 82

delete Q8203.

delete C8207.

change CE8202 to 11G08D2227D1 from 11G09X222755.

change U8201.7, U8201.15, R8205.1 to SGND.

page 83

change CE8301 to 11G08D2227D1 from 11G09X222755.

change JP8301 to 2MM.

page 88

change U8801.6 net name to CHG\_INE3 from CHG\_COMP3.

change C8806, C8809 to 11G233115214320 from 11G23210412360.

change Q8802, Q8803 PCB Footprint to soic\_8p\_50\_197x236.

page 91

change R9107 to 10G212220214030 from 10G213220213010.

page80

add net name "SNB\_PH1" between R8020 and C8040

add net name "SNB\_PH2" between R8021 and C8041

change C8040 to 11G232115214320 from 11G233115214320.

change C8041 to 11G232115214320 from 11G233115214320.

page 84

change JP8402.1 connection to +1.8V from +1.8V0

add net name "5930\_VIN" on U8401.5 and U8401.9

change net name "5913\_FB" to "5930\_FB" on U8401.2

page 88

add net name "SNB\_CHG" between R8804 and C8803

add net name "CHG\_BST" between R8810 and C8802

change C8803 to 11G232115214320 from 11G233115214320.

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<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K40IJ/K50IJ</b>	1.1	
Date: Monday, March 09, 2009		Sheet	78 of 98

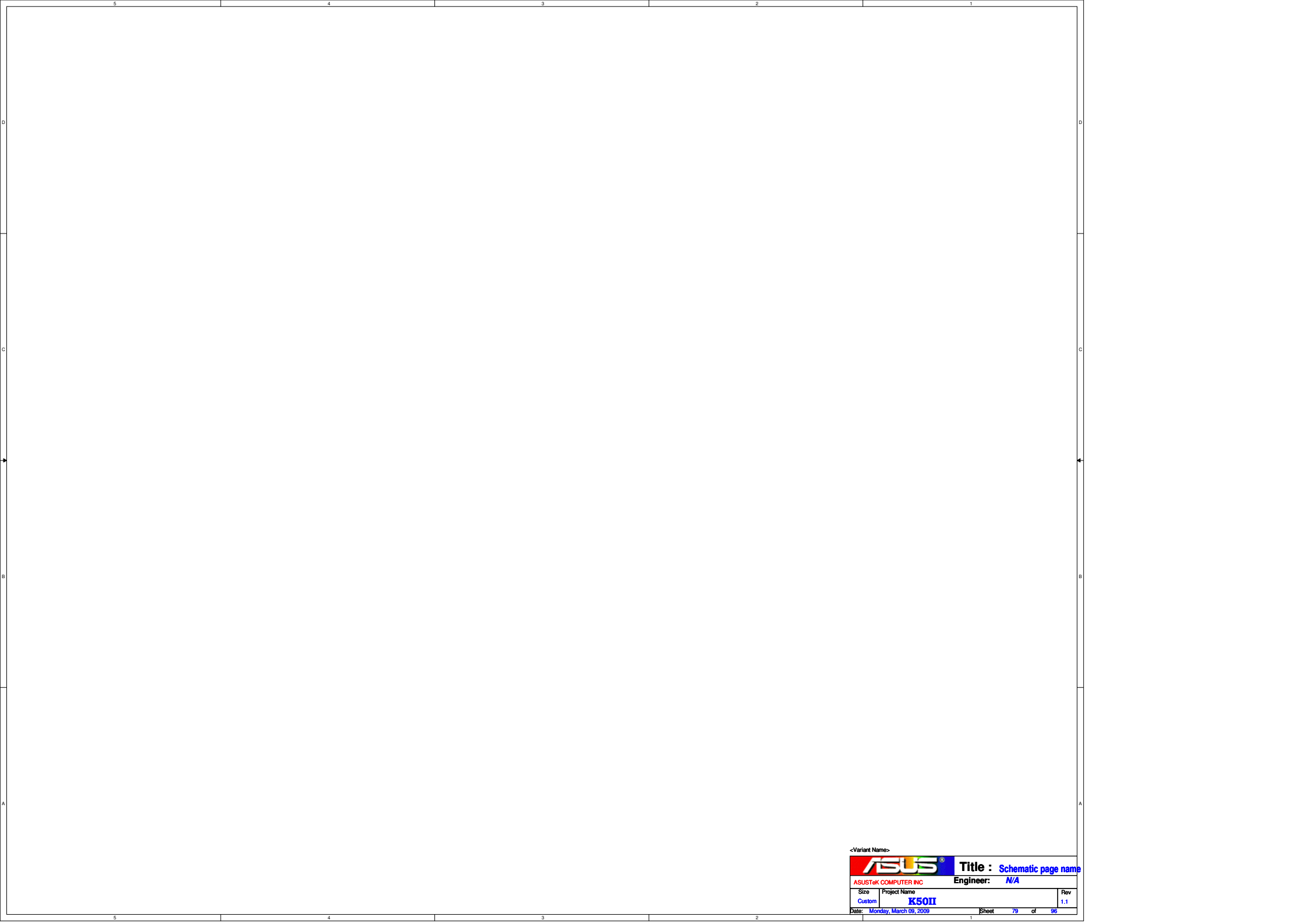
5

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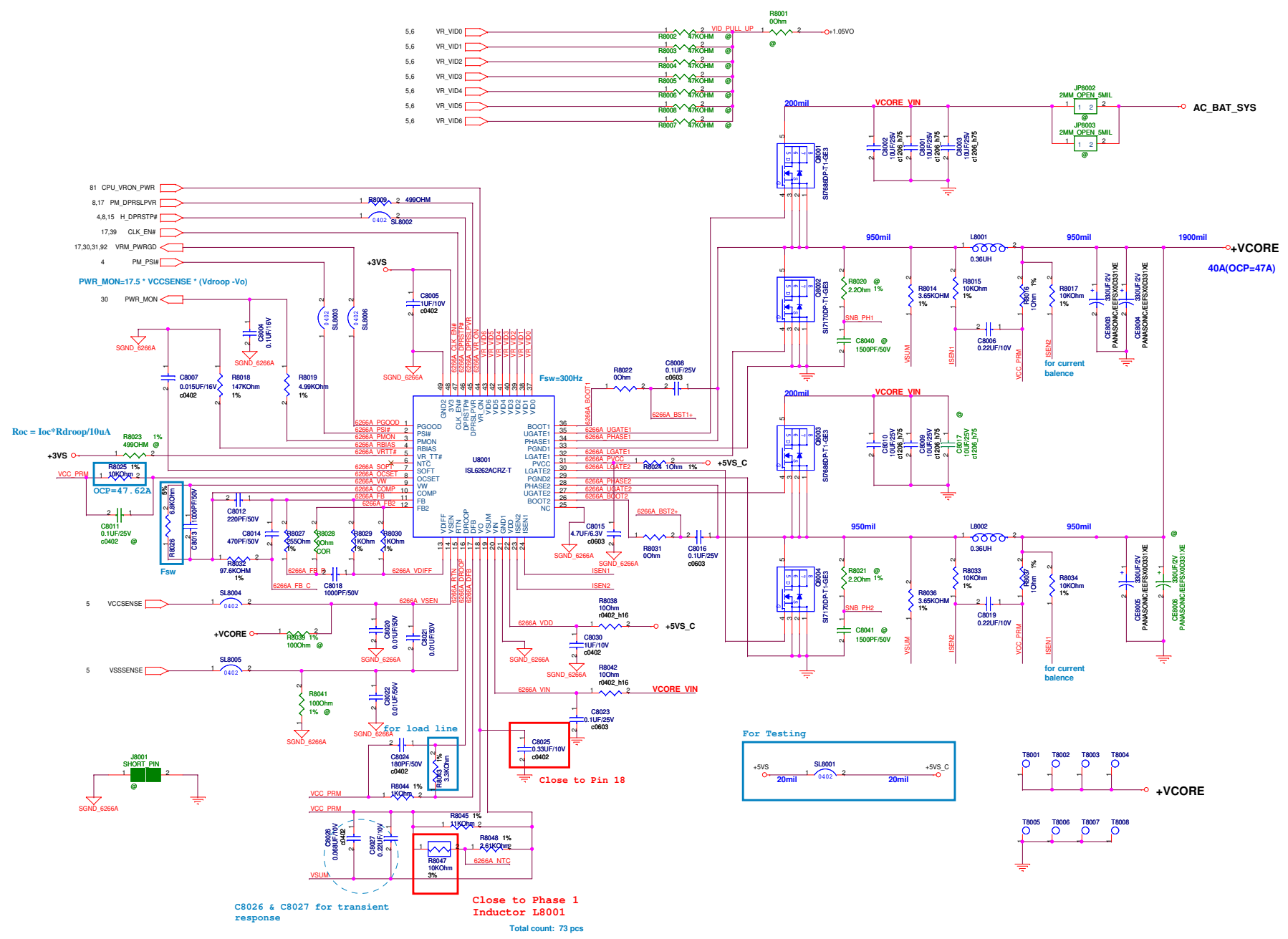
2

1



<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	<b>K50II</b>	1.1	
Date: Monday, March 09, 2009		Sheet	79 of 96

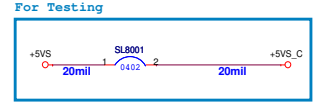


$Roc = Ioc * Rdroop / 10uA$

OCP = 47.62A

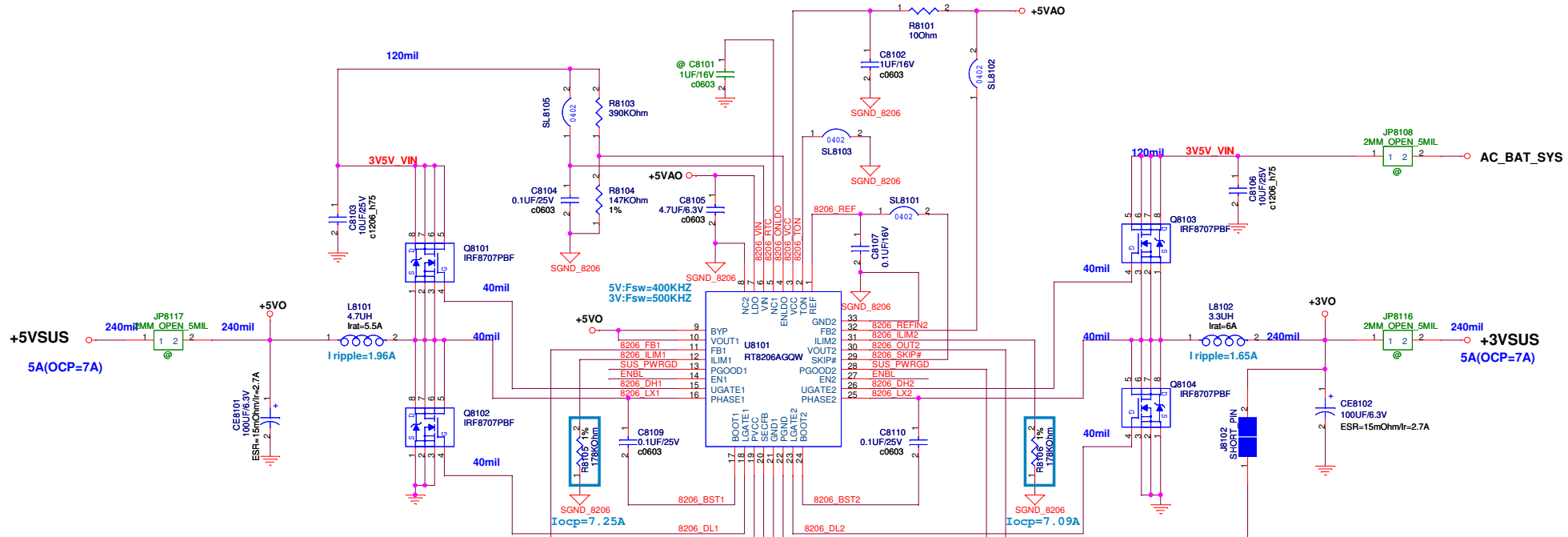
Fsw = 300kHz

Close to Phase 1 Inductor L8001  
Total count: 73 pcs

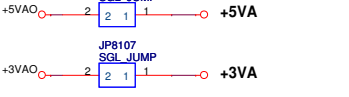
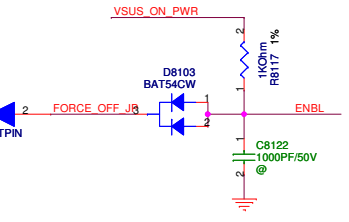
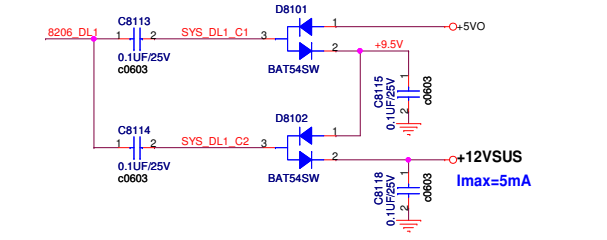
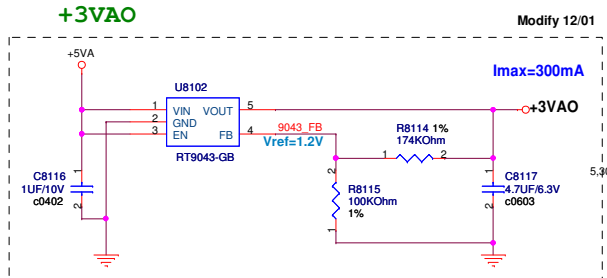


HS MOS Second source IRF8714  
 LS MOS Second source IRF8736

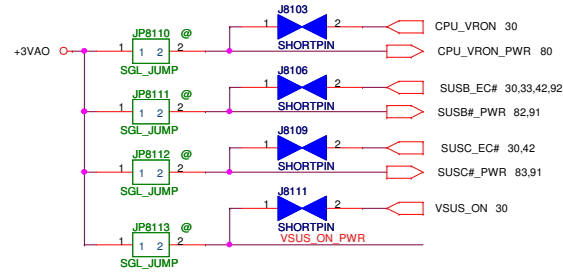




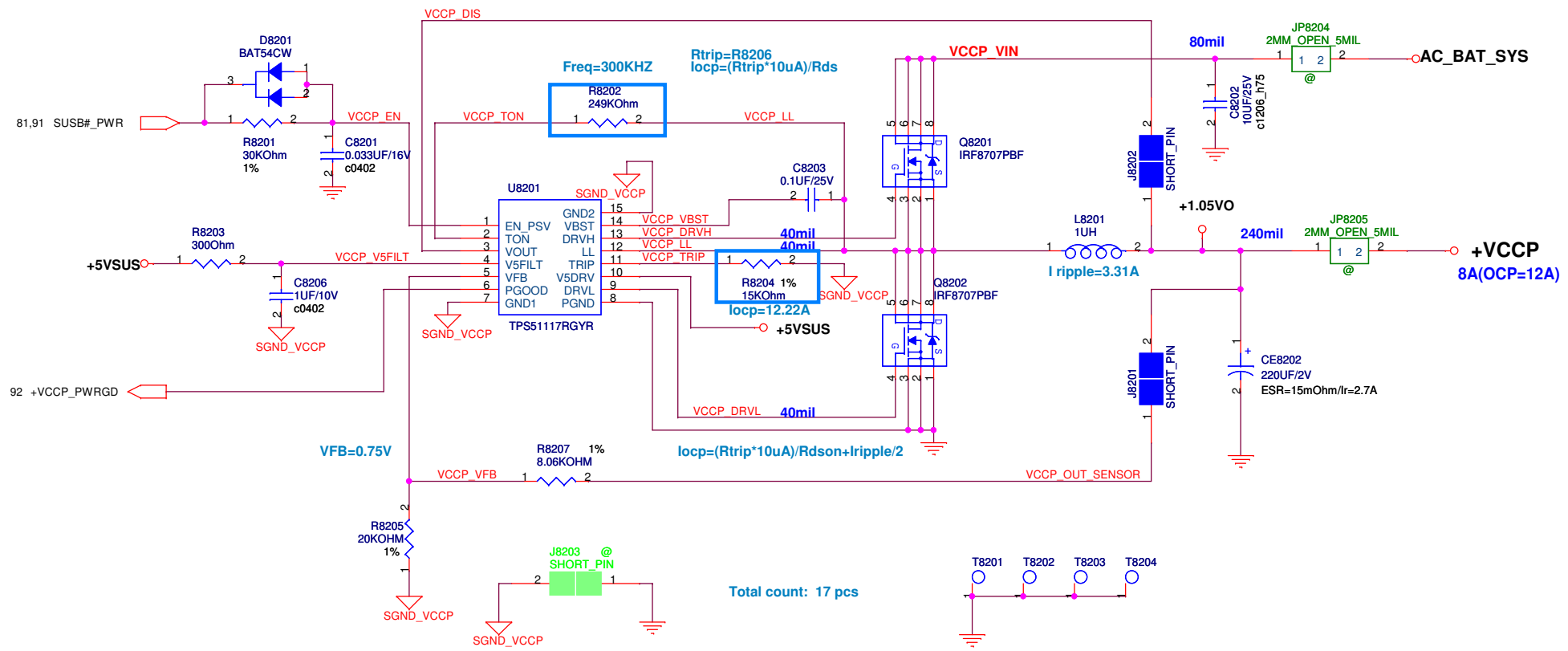
$$I_{ocp} = (R_{ilim} * 5\mu A) / 10 / R_{ds(on)} + I_{ripple} / 2$$



**FOR POWER TEST**

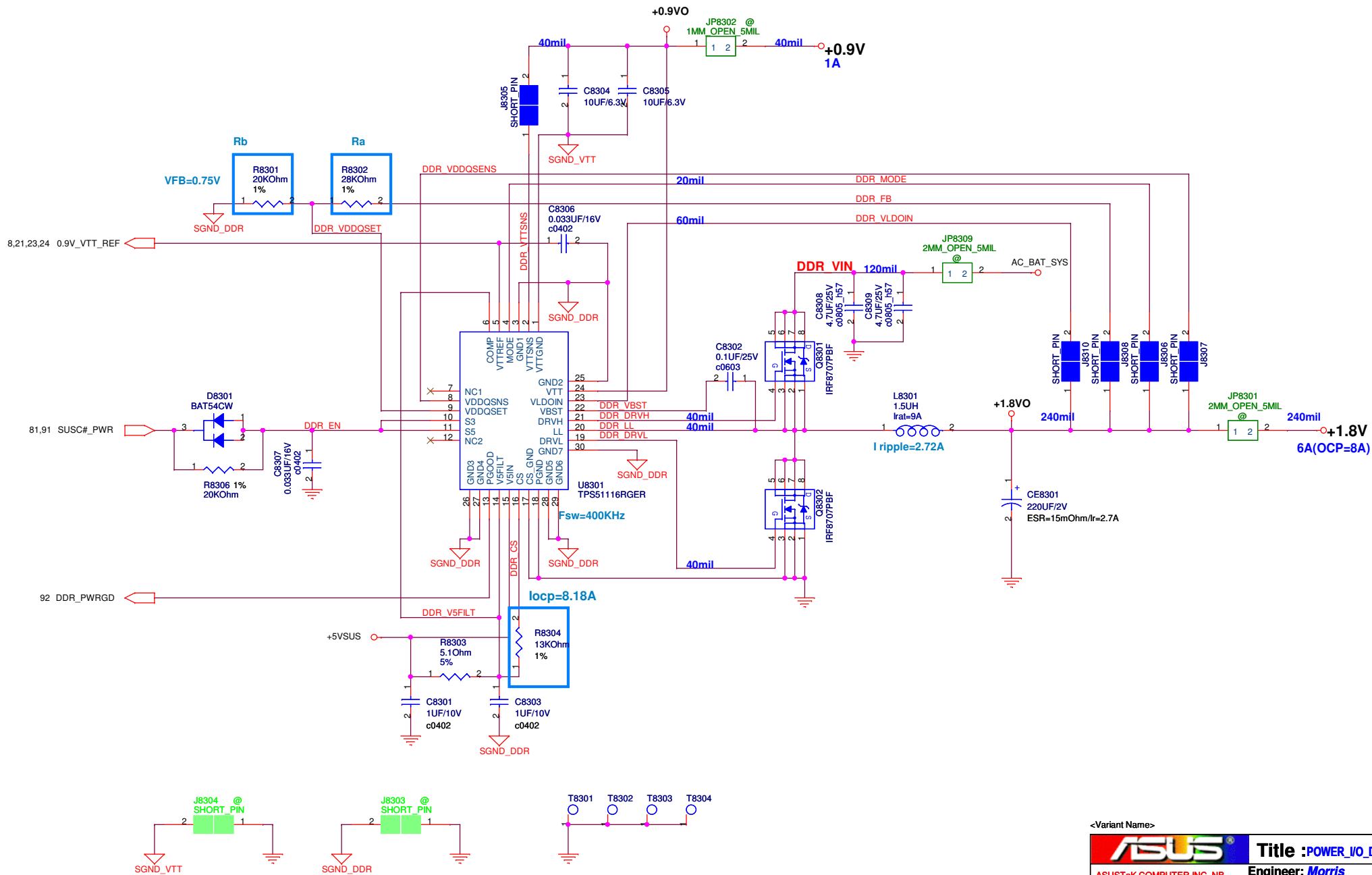


Total count: 44 pcs



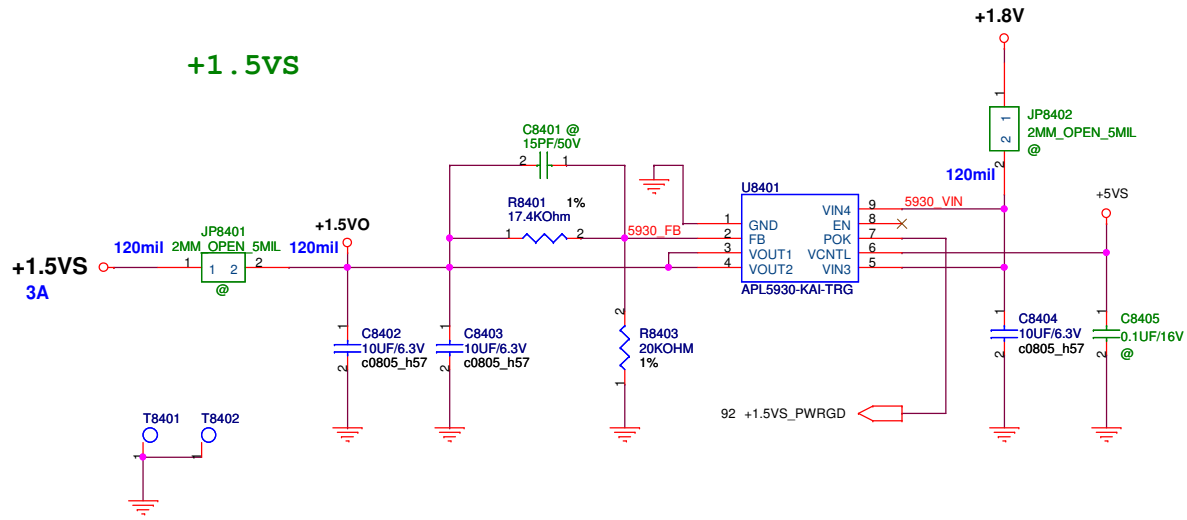
<Variant Name>

<b>ASUS</b>		<b>Title :POWER_I/O_+VCCP</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <b>Morris</b>	
Size	Project Name	Rev	
Custom	<b>K50</b>	1.0	
Date: Monday, March 09, 2009	Sheet 82	of 96	



<Variant Name>

<b>ASUS</b>		<b>Title :POWER_I/O_DDR</b>
ASUSTeK COMPUTER INC. NB		Engineer: <b>Morris</b>
Size B	Project Name <b>K50</b>	Rev 1.0
Date: Monday, March 09, 2009		Sheet 83 of 96



Total count: 7 pcs

<Variant Name>

		<b>Title :</b> POWER_IO_+1.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size B	Project Name <b>K50</b>	Rev 1.0	
Date: Monday, March 09, 2009		Sheet	84 of 96

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<Variant Name>



Title :

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
A		1.0

Date: Monday, March 09, 2009

Sheet 85 of 96

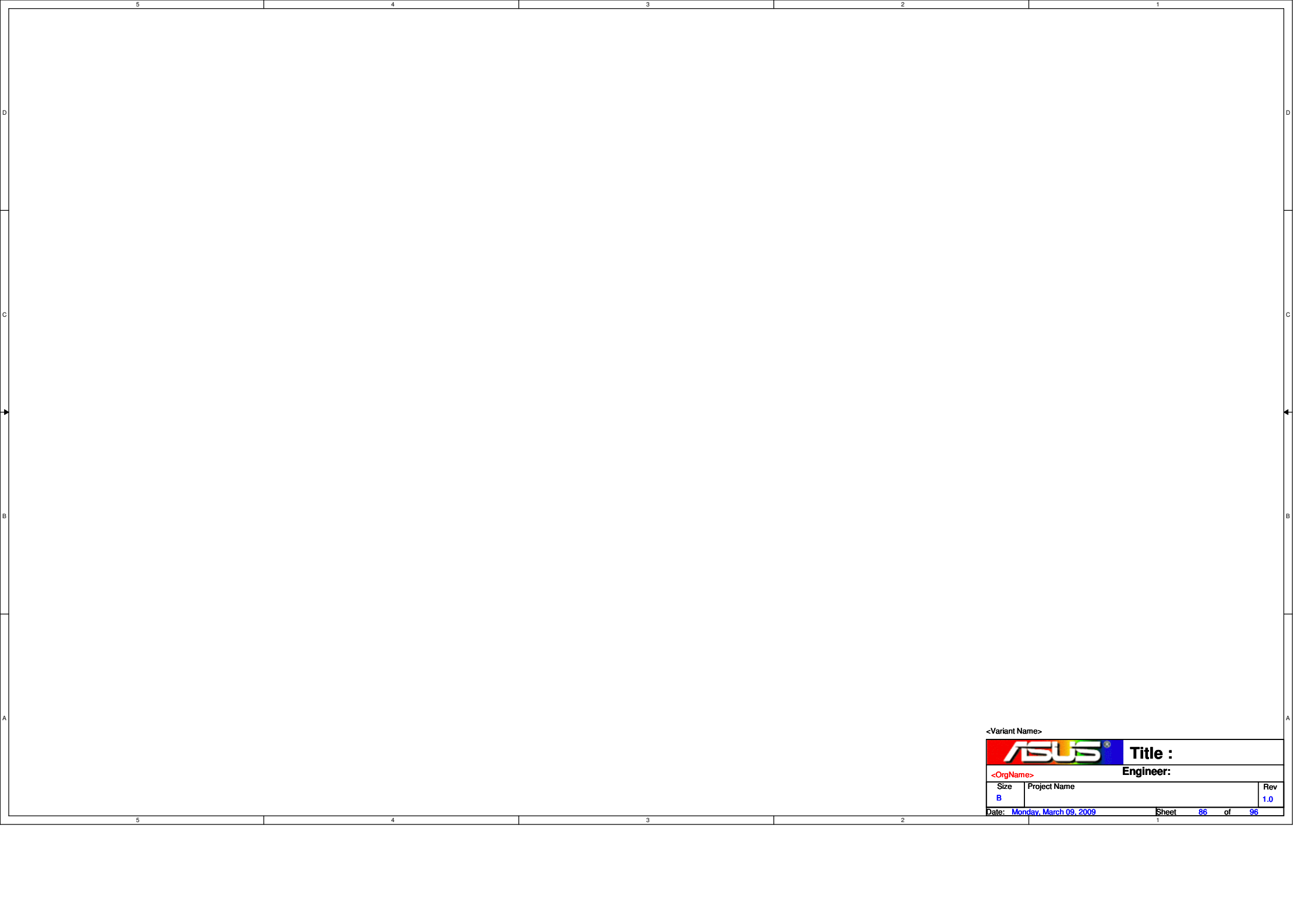
5


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<Variant Name>		
		<b>Title :</b>
<OrgName>		<b>Engineer:</b>
Size	Project Name	Rev
B		1.0
Date: <a href="#">Monday, March 09, 2009</a>		Sheet <a href="#">86</a> of <a href="#">96</a>

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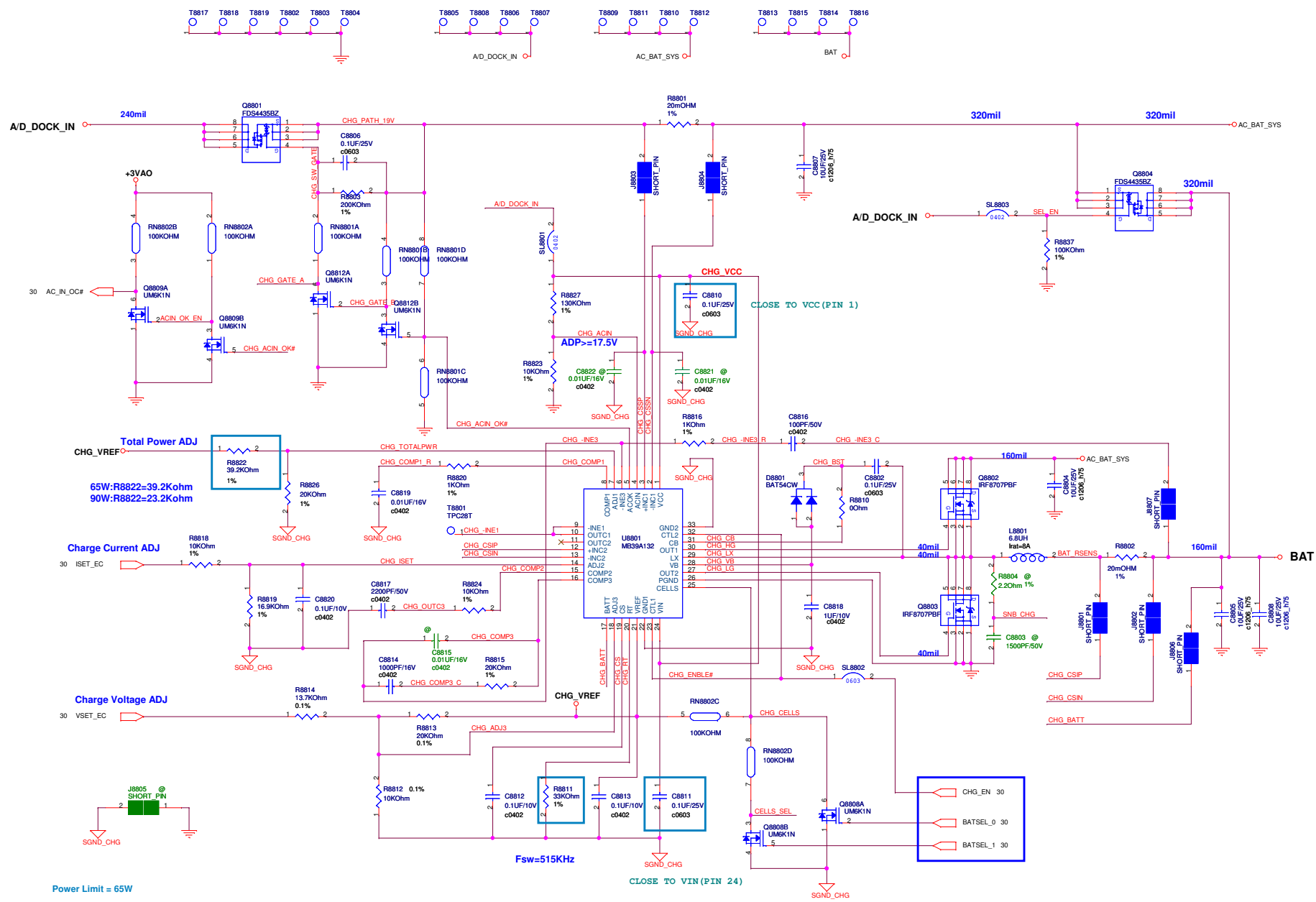
<Variant Name>



<OrgName>		Engineer:
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Size	Project Name	Rev
Custom		1.0

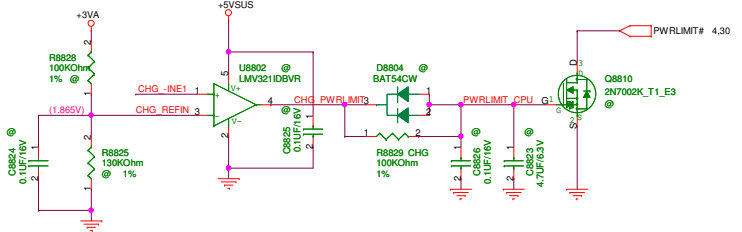
Date: Monday, March 09, 2009 Sheet 87 of 96



TOTAL COUNT:56 PCS

Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :  
 Charger MAX8725 => EC CODE : 200  
 Charger MAX17015 => EC CODE : 201  
 Charger MB39A132 => EC CODE : 202





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<Variant Name>

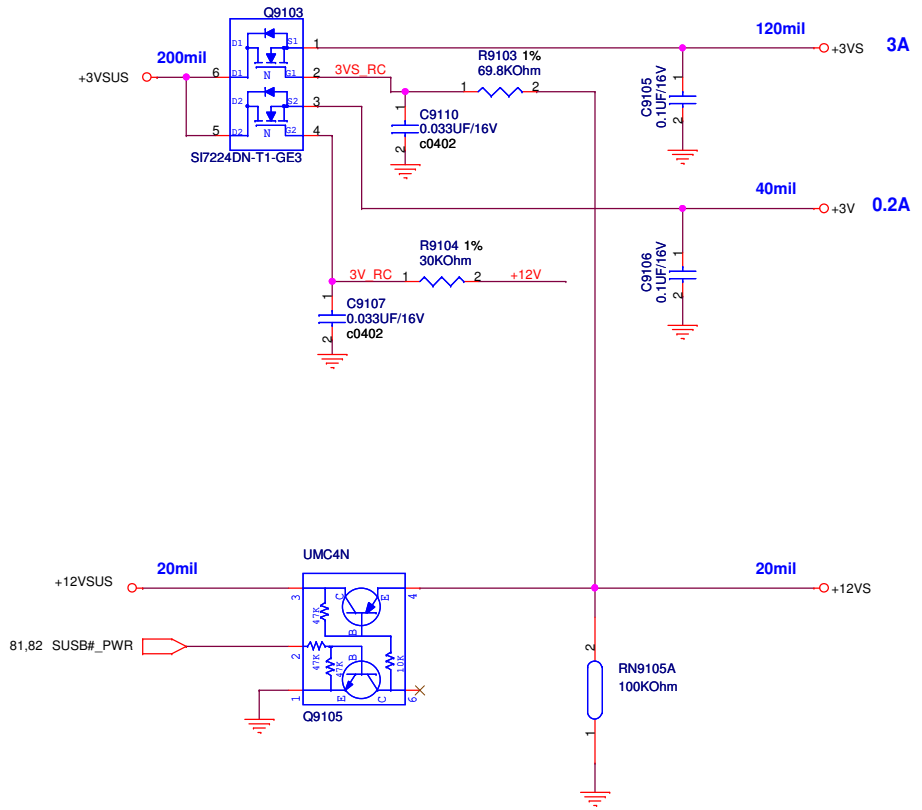
		<b>Title :</b>	
<OrgName>		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom		1.0	
Date: Monday, March 09, 2009		Sheet 89 of 96	

BATTERY IN DETECT

<Variant Name>

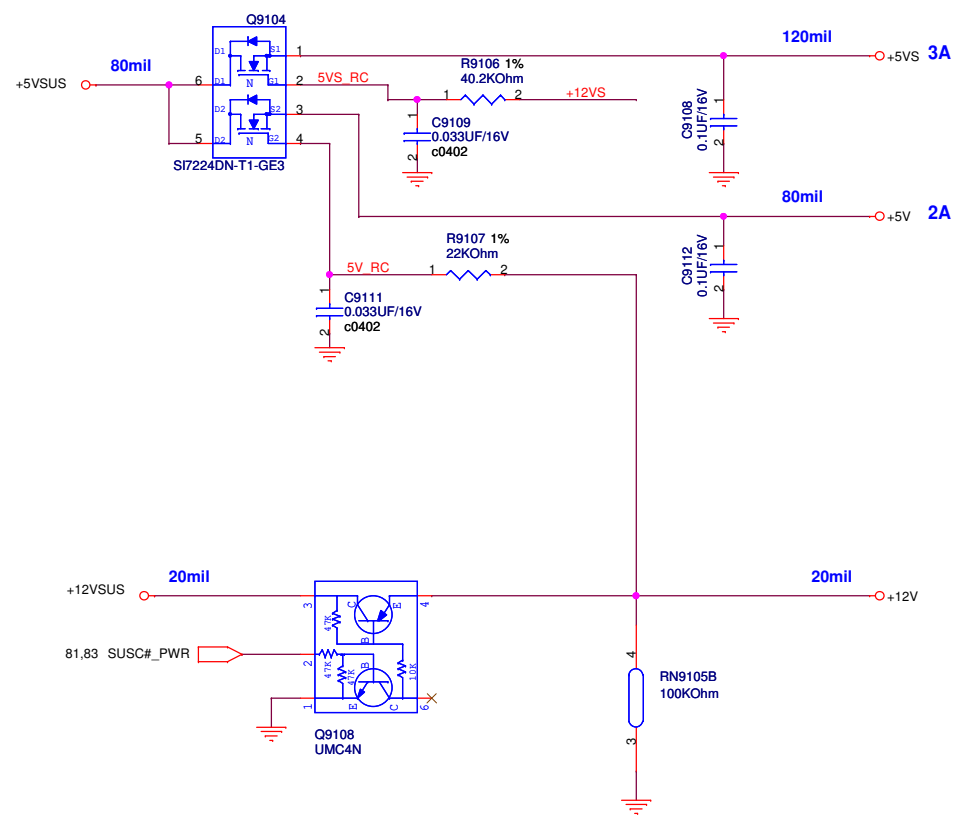
		<b>Title : POWER_DETECT</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
Custom	<b>K50II</b>	1.0	
Date: Monday, March 09, 2009		Sheet	90 of 96

# SUSB#\_PWR POWER



Total count: 19 pcs

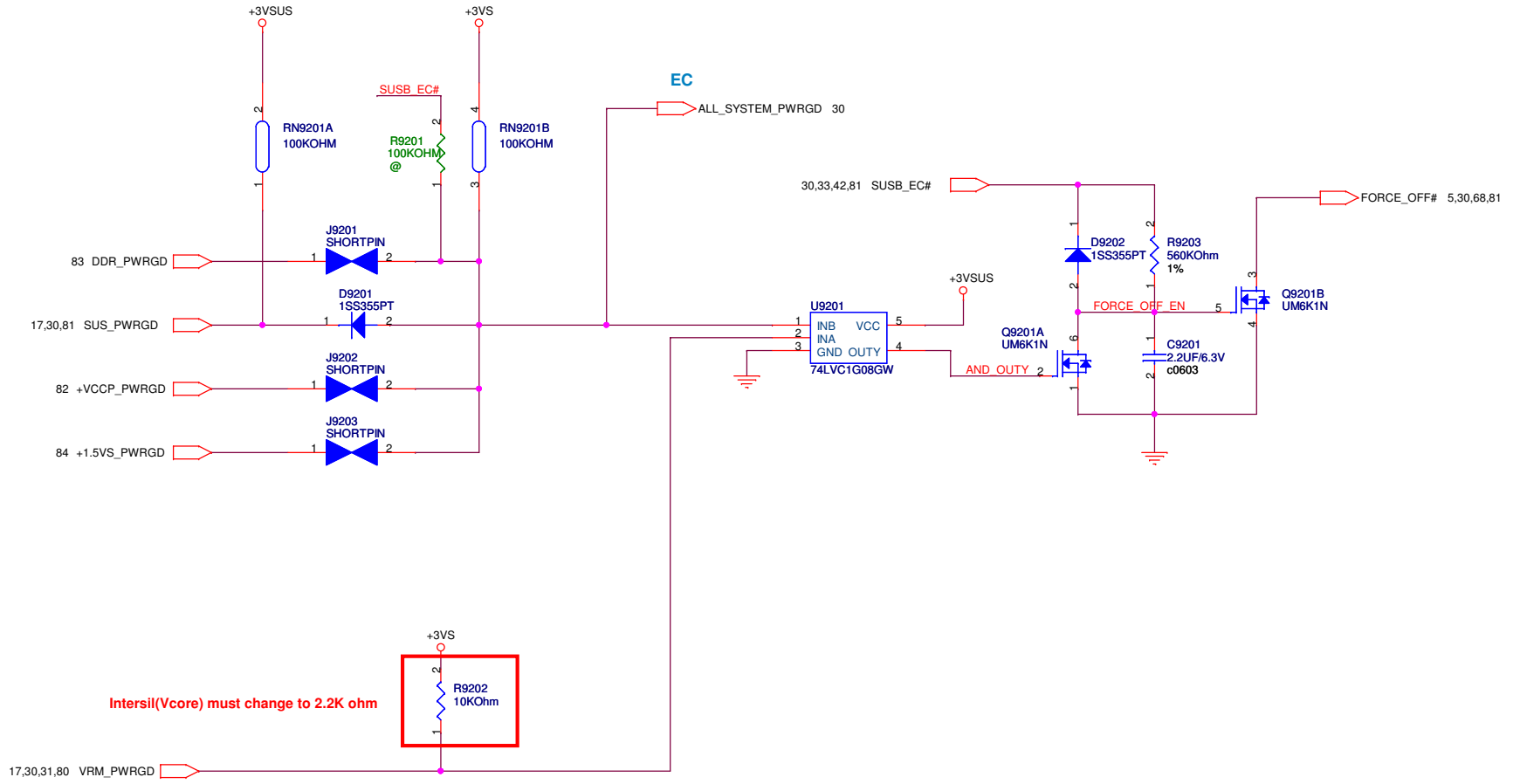
# SUSC#\_PWR POWER



<Variant Name>

<b>ASUS</b>		<b>Title :POWER_LOAD SWITCH</b>
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>
Size B	Project Name <b>K50</b>	Rev 1.0
Date: Monday, March 09, 2009		Sheet 91 of 96

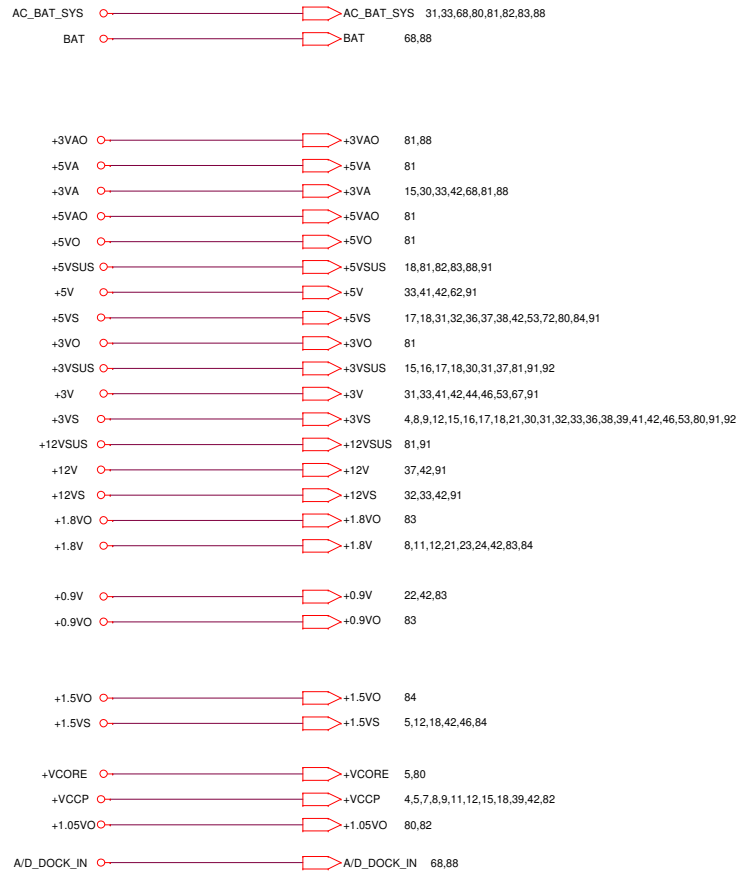
# POWER GOOD DETECTOR



Total count: 8 pcs

<Variant Name>

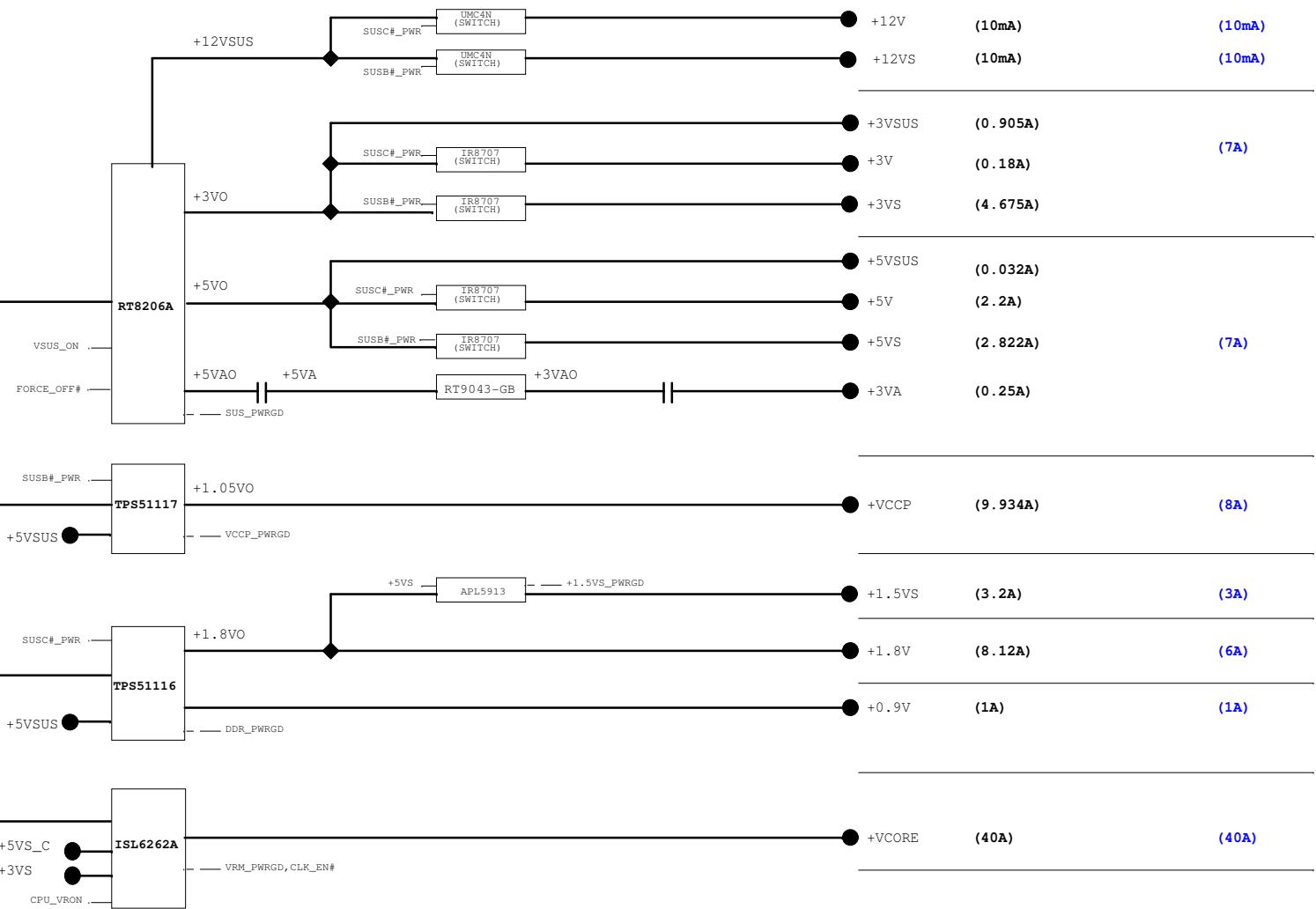
		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Morris	
Size B	Project Name K50	Rev 1.0	
Date: Monday, March 09, 2009		Sheet	92 of 96



<Variant Name>

		<b>Title : POWER_SIGNAL</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
Custom	<b>K50</b>	1.0	
Date: Monday, March 09, 2009		Sheet 93 of 96	

AC\_BAT\_SYS



K50  
Non-IAMT  
Design rating

Voltage	Current	Design rating
+12V	(10mA)	(10mA)
+12VS	(10mA)	(10mA)
+3VSUS	(0.905A)	(7A)
+3V	(0.18A)	
+3VS	(4.675A)	
+5VSUS	(0.032A)	
+5V	(2.2A)	
+5VS	(2.822A)	(7A)
+3VA	(0.25A)	
+VCCP	(9.934A)	(8A)
+1.5V	(3.2A)	(3A)
+1.8V	(8.12A)	(6A)
+0.9V	(1A)	(1A)
+V CORE	(40A)	(40A)

VR\_VID0~VR\_VID6, H\_DPRSTP#,  
MCH\_OK, PM\_DPRSLEPR, PM\_PSI#,  
VCCSENSE, VSSSENSE, STP\_CPU#,  
PWR\_MON